

COMPAL CONFIDENTIAL

MODEL NAME : HDL51
PCB NO : DA8001S4000
PCB 2X2 LA-L947P REV0 M/B 1 S

ADL-P+NPCX996D
(DIS)
2022-4-11
REV : 1.0 (A00)

ADL CPU QS

UC1
SA0000FE10L
I5-1235U
Q0EQ@
(no 12W, no-IPU)
S IC A31 FJ8071504826803 Q0EQ R0 1.3G S

UC1
SA0000FB71L
I5-1235U
Q0EP@
S IC A31 FJ8071504826802 Q0EP R0 1.3G S

UC1
SA0000FB51L
I7-1255U
Q0E8@
S IC A31 FJ8071504826607 Q0E8 R0 1.7G S

ADL CPU Base-U

ADL CPU R3

UC12
SA0000FB73L
RLFQ@
S IC FJ8071504826802 SRLFQ R0 1.3G A31 !

UC13
SA0000FB53L
RLFQ@
S IC FJ8071504826607 SRLFP R0 1.7G A31 !

@ : Un-pop Component
UMA@/DIS@ : If support external Graphic card
N3@/V3@ : Inspiron/Vostro
MSFT@/NMSFT@ : MSFT SKU / Normal SKU
G3@ : Support G3 sharing SPI topology
CNV@ : Support CNVi function
S5LID@/LID@ : Support S5 LID power up Function/Normal LID close
I2CTCH@/USBTCH@ : Touch Screen support I2C signal / USB signal
BASE@/PREM@ : Pentium,Celeron/i3,i5,i7
I2CPAD@/PS2PAD@ : EC use I2C touch PAD signal(or PS2)
JP@/JUMP@/PJP@ : JUMP
100@/1000@ : 10/100 LAN / Giga-LAN
PRO@/ICPRO@ : only LCDVDD protection/Hinge up protection Support
EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
KBBL@ : KB Backlight
TPM@/NTPM@ : HW TPM/SW TPM
750_CTPM@ : 750 and china TPM
CTPM@/ST_CTPM@ : China TPM/ST China TPM
FFS@ : Free Fall Sensor
TYPEC@/NTYPEC@ : Support TypeC/non-TypeC
TYPEC@EMI@/TYPEC@ESD@ : EMI, ESD ,TypeC Component
LBIST@/LBIST@RF@ : LBIST for LCD monitor
TP@/CMC@TP@ : Test Point/XDP Test Point
DISPCB@/UMAPCB@ : PCB MB

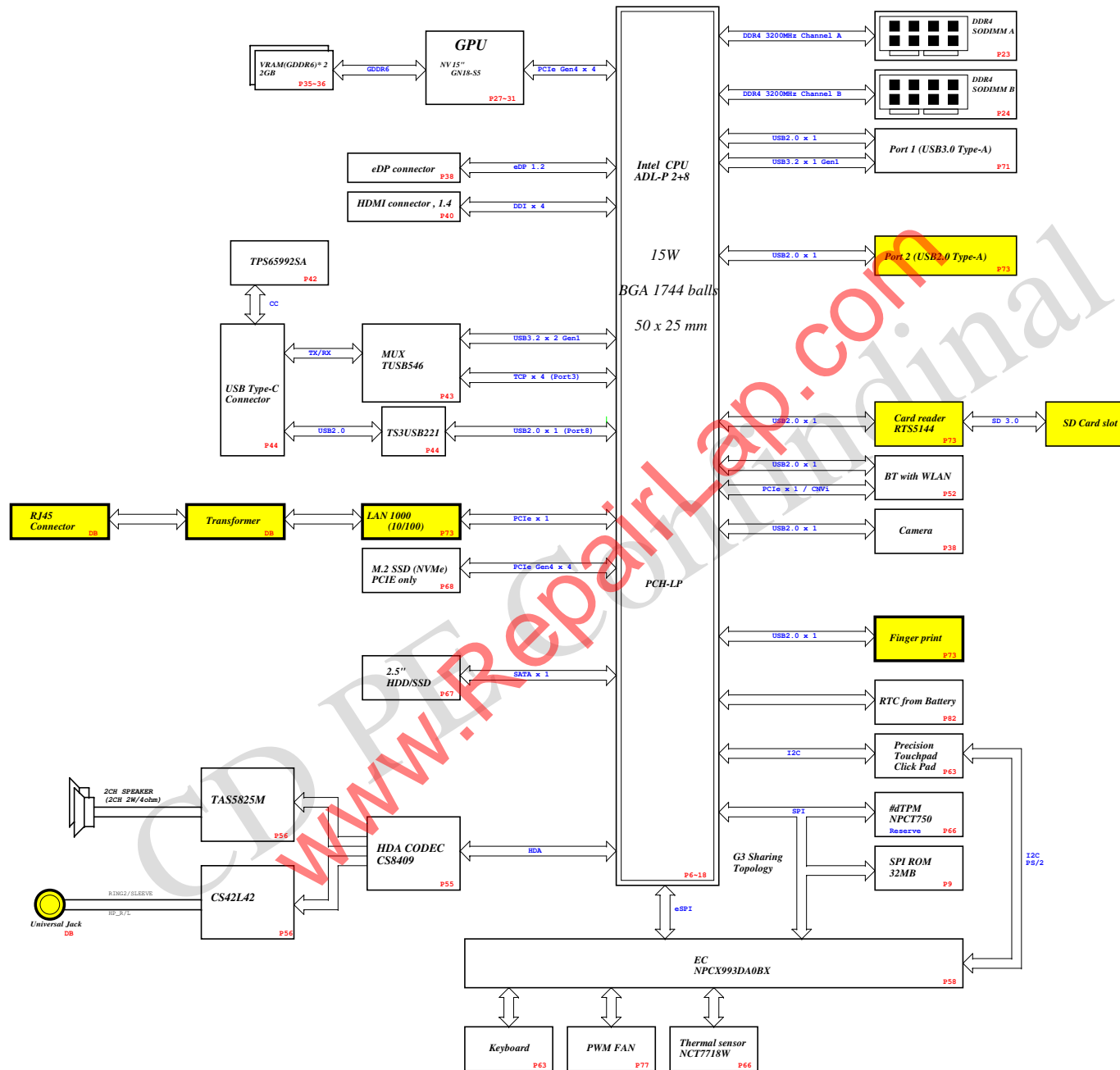
Layout Dell logo



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PWB: 9HTP8

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Block Diagram



Battery	RTC
Charger	Daughter board

Security Classification	Confidential	Compal Secret Data	20190401	20190401
Issued Date	20190401	Declassified Date	20190401	20190401
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LA-1947P				
Version: 1.0				

POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

Voltage Rails

Power Plane	Description	S0	S3	S4/S5	G3
+19V_ADPIIN	Adapter power supply	N/A	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A	N/A
+RTC_SOC	RTC power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*	OFF
+5VALW	System +5V always on power rail	ON	ON	ON*	OFF
+3VALW	System +3V always on power rail	ON	ON	ON*	OFF
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*	OFF
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6V power rail for DDR terminator	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	ON	ON	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF	OFF
VCCPLL	+1.05 VCCPLL power rail	ON	ON	ON	OFF
+VCC_IN	Core voltage for CPU	ON	OFF	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	OFF
+3VALW_DSW	+19VB to DSW power rail for suspend power	ON	ON	ON	OFF
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*	OFF
+5VS	System +5VS power rail	ON	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF	OFF
+1.35V_MEM GFX	+1.35V power rail for GPU	ON	OFF	OFF	OFF
+3VGS	+3V power rail for GPU	ON	OFF	OFF	OFF
+1.8VGS	+1.8V power rail for GPU	ON	OFF	OFF	OFF
+0.95VSDGPU	+0.95V power rail for GPU	ON	OFF	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

RE: ICL N3V3 MLK High Power Consumption on VCCIN_AUX Under S3/S5

Wu, Eddie <eddie.wu@intel.com>

发件日期: 2019/5/6 (周四) 下午 09:41

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副本: Chen, AlexCL (TPE); Chang, Gary; Hsiao, Jimmy

Hi David,
VCCIN_AUX only down to 0V while SLP_S0# is asserted.
On S3 mode, it only can down to 1.1V. Thanks.

Best Regards,
Eddie Wu +886-2-66221110

USB 2.0	DESTINATION
1	USB2.0 port1
2	NC
3	USB2.0 port3, IO/B
4	Type-C
5	Finger printer
6	CCD
7	Card reader , IO/B
8	NC
9	NC
10	BT

Board ID & Model ID Table

Bullseye TGL			
NBDR	SKU	Model-ID (RE4 PD-100K)	Board-ID (RE2 PD-100K)
	UMA	RE3 PU-10K	RE1 PU-10K -EVT RE1 PU-17.8K -DVT1 RE1 PU-27.0K -Reserve RE1 PU-37.4K -DVT2 RE1 PU-49.9K -Reserve RE1 PU-64.9K -Pilot RE1 PU-82.5K -Reserve
	DSC - N175-G3	RE3 PU-17.8K	

10.12.4 Power States

Table 207. System with M3 State Supported

Rails	SKUs	S0/M0 3	C102	S0ix/M-off*	S3/M3	S3/M-off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3†
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_VNNEXT_1 P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_V1P05EXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M5	All	ON	ON	OFF	ON ¹⁰	OFF	ON ¹⁰	OFF	OFF	No Power
V1.8M5	All	ON	ON	OFF	ON ¹⁰	OFF	ON ¹⁰	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST	All	ON	ON	ON	ON ¹³	ON ¹³	OFF ⁵	OFF ⁵	OFF	No Power
VCCSTG	All	ON	OFF ²	OFF	OFF	OFF	OFF	OFF	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON ¹¹	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON ¹¹	OFF ¹⁴	OFF ¹⁴	OFF ¹⁴	OFF ¹⁴	OFF	No Power

Note : VCCIN_AUX only down to 0V while SLP_S0# is asserted. On S3 mode, it only can down to 1.1V.

Processor PCIe												PCIe											
1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	5	6	7	8	9	10	11	12
PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie	PCie
PCie X4 Gen4				PCie X4 Gen4				X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1
dGPU(GN18-S5)				M.2 SSD Gen4				1	M/B USB-A	M/B USB-A	M/B USB-A	M.2 SSD Gen3				2	LAN	WLAN	HDD				

USB/DDI															
Processor USB				USB 2.0										DDI	
1	2	3	4	1	2	3	4	5	6	7	8	9	10	1	2
TCP	TCP	TCP	TCP	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	DDI A	DDI B
TBT/USB4			TBT/USB4	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	eDP	HD MI
		Type-C DP	M/B USB-A	M/B USB-A	M/B USB-A IO/B	Type-C	Finger print	Camera	Card reader				BT	LCD	HDMI

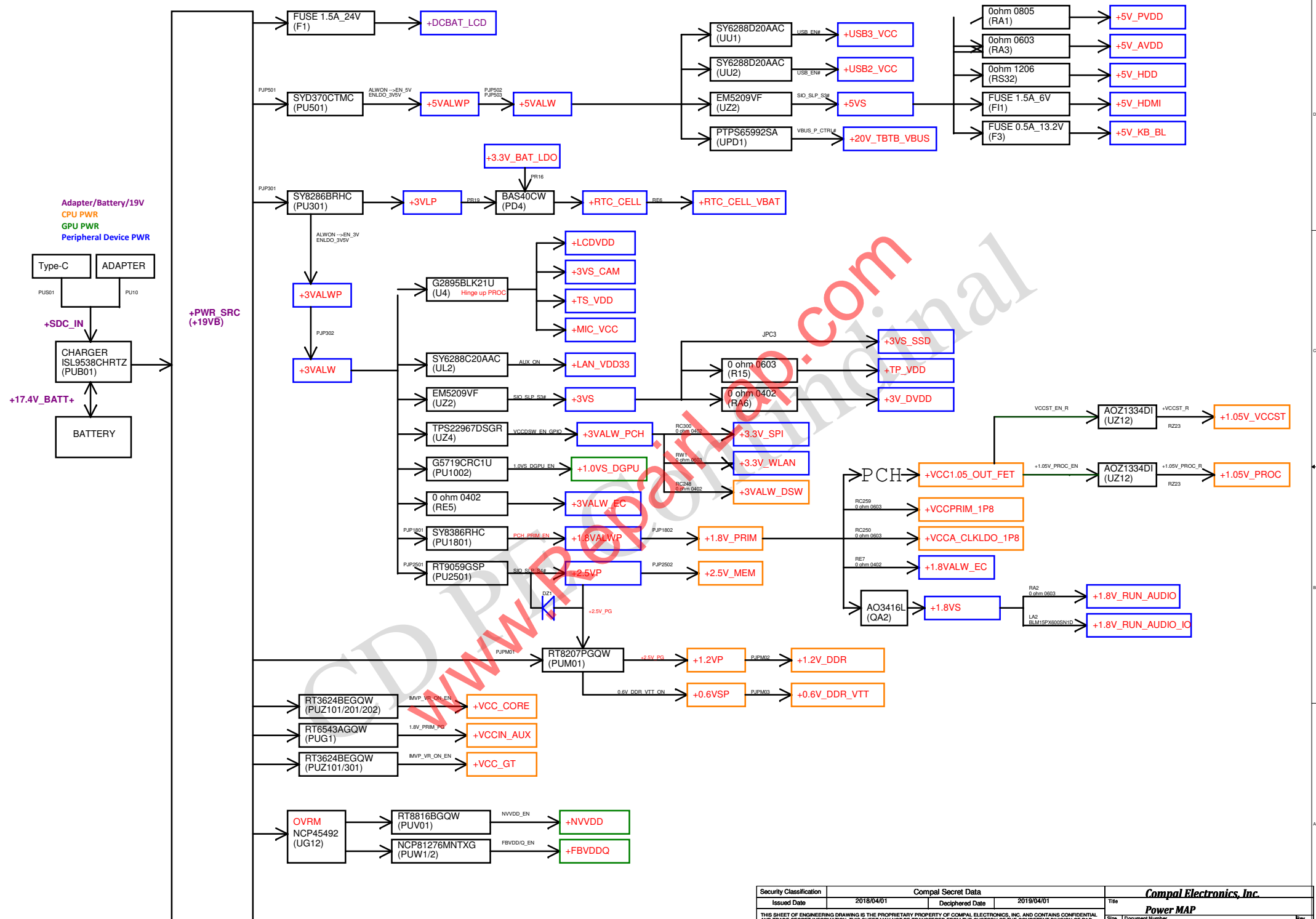
1. Only for UMA/DSC(8L)
2. Only for UMA(6L)

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 (MB)(Type-A)
USB3.0-2	PCIE-2		NC
USB3.0-3	PCIE-3		USB3.0 (MB)(Type-C)
USB3.0-4	PCIE-4		NC
	PCIE-5		NC
	PCIE-6		NC
	PCIE-7		NC
	PCIE-8		NC
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1	NC
	PCIE4A - 0		GPU
	PCIE4A - 1		GPU
	PCIE4A - 2		GPU
	PCIE4A - 3		GPU
	PCIE4B - 0		PCIE SSD
	PCIE4B - 1		PCIE SSD
	PCIE4B - 2		PCIE SSD
	PCIE4B - 3		PCIE SSD

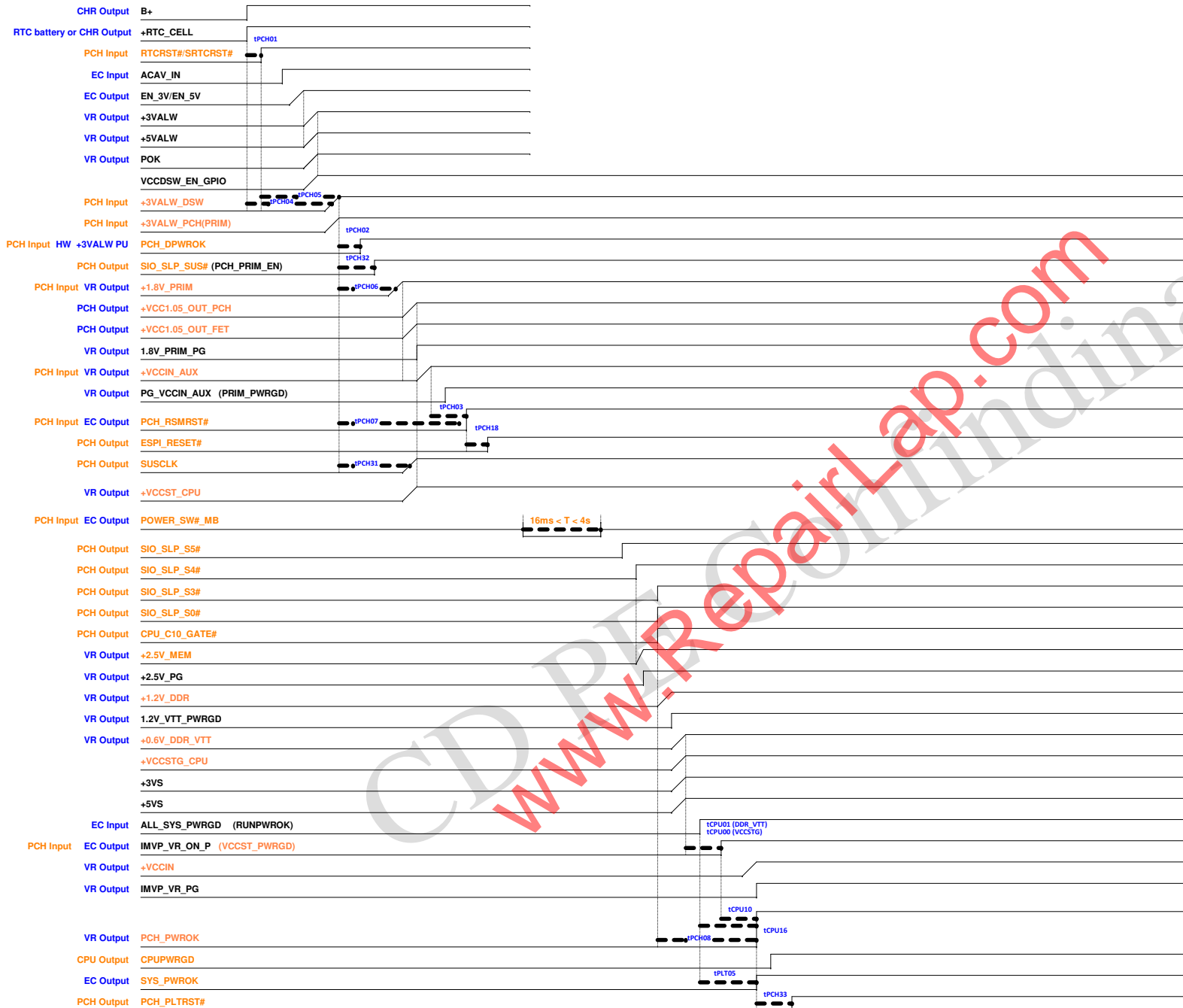
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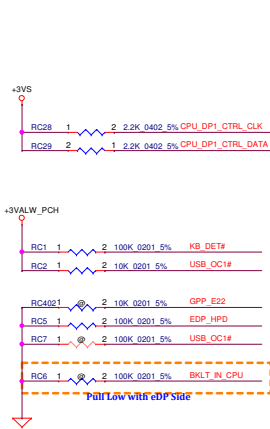
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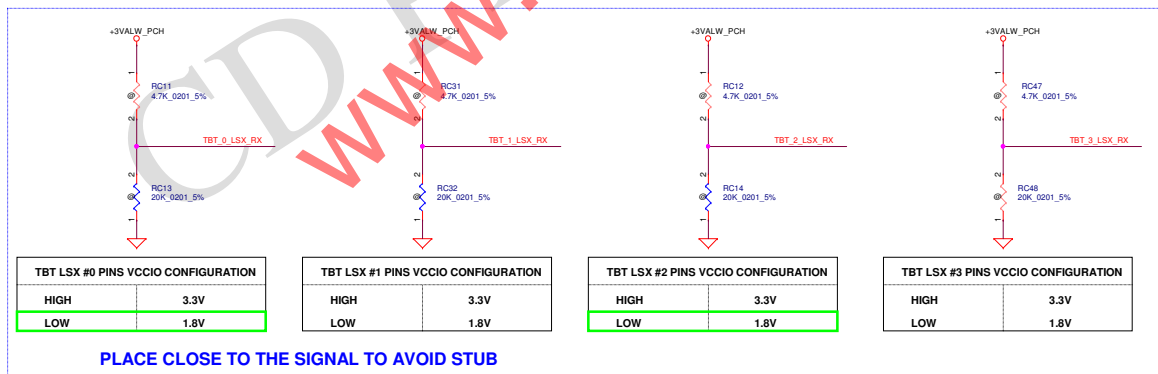
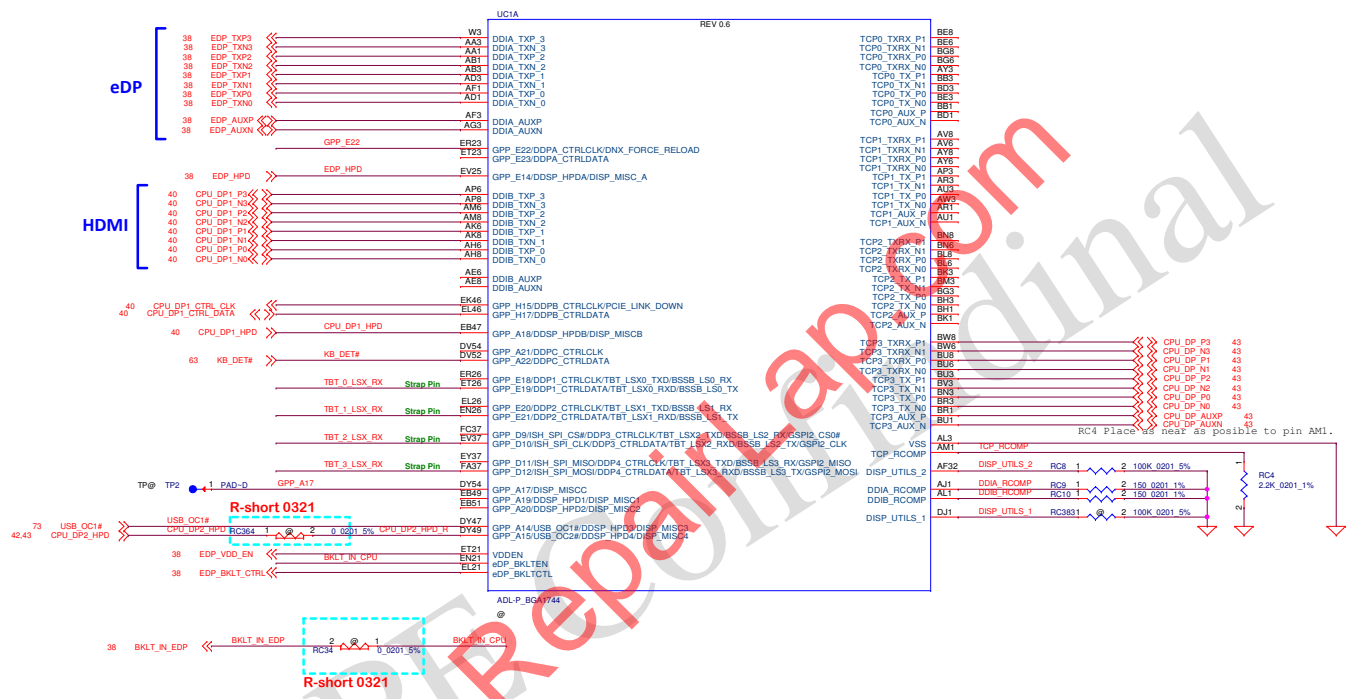


Power Up Sequence
G3 to S0

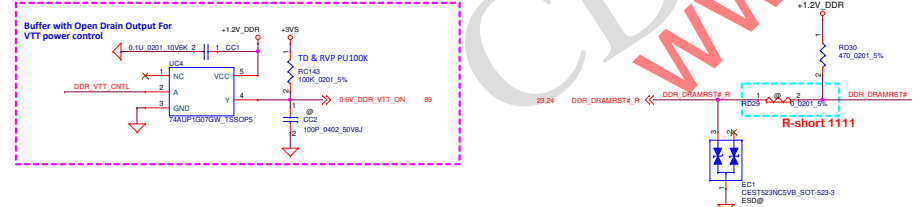
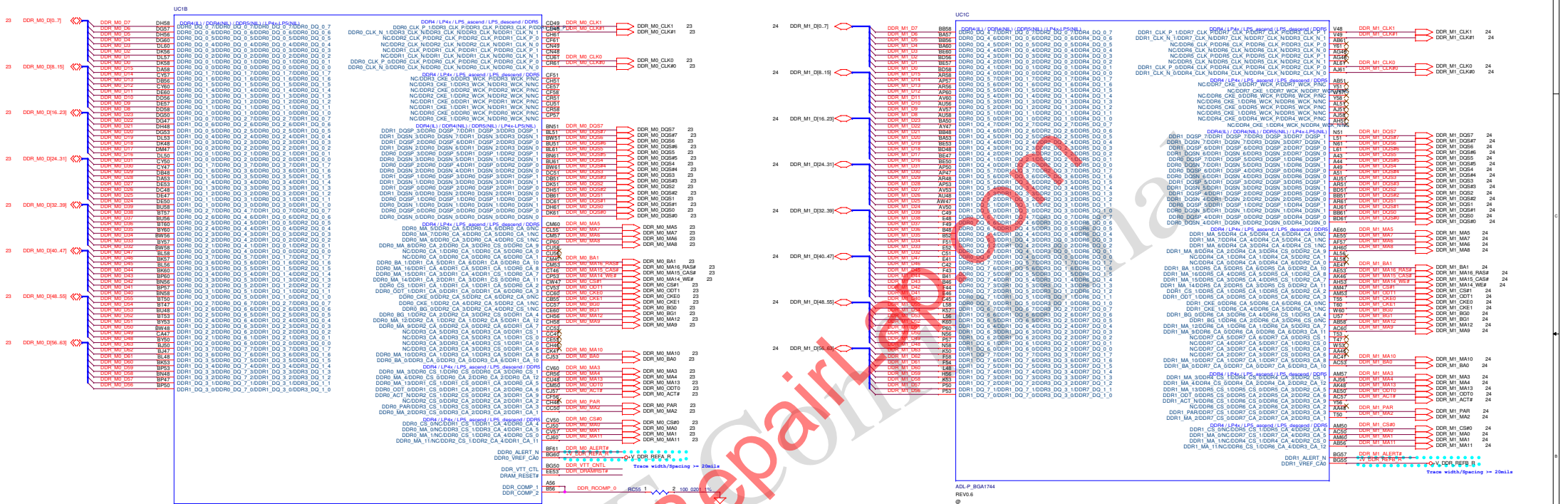




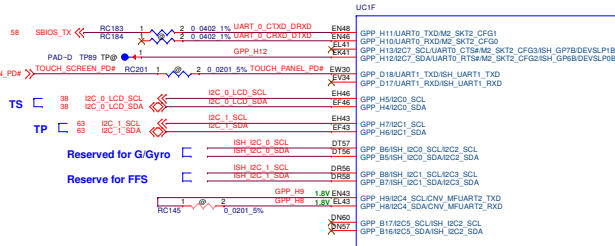
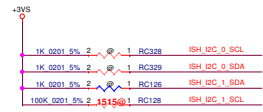
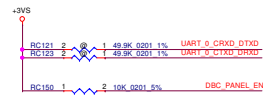
GPIO	DEVICE CONTROL
USB_OC0#	USB Port (MB)
USB_OC1#	USB Port (IO)
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	HDD
DEVSLP1	NA
DEVSLP2	M.2 SSD



PLACE CLOSE TO THE SIGNAL TO AVOID STUB

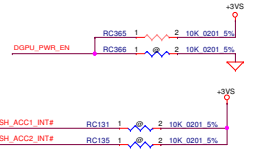
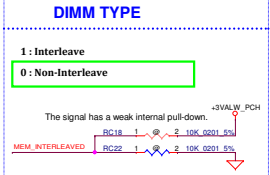
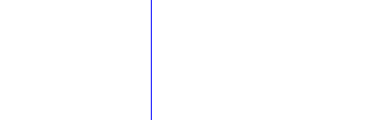
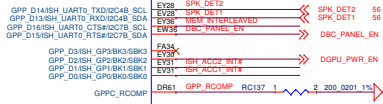


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Date: Friday, April 08, 2022				10mm	8 of 121

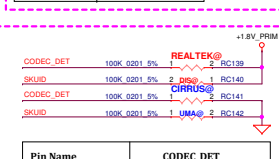
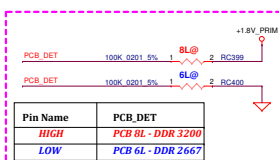
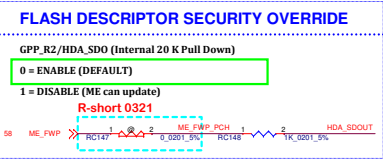
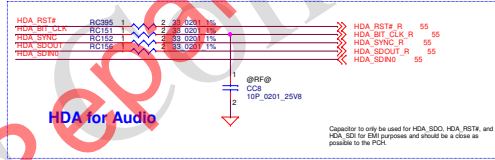


ISH_GPIO for Main Accelerometer (KB Board)INT#
 ISH_GPIO for 2nd Accelerometer (Camera Board)INT#
 ISH_GPIO for TABLE_MODE#
 ISH_GPIO for A.S. ALERT#
 ISH_GPIO for NB_MODE#(N/A)
 ISH_GPIO for NB_LDR(N/A)
 ISH_GPIO for TAB_LDR(N/A)
 ISH_GPIO for Proximity sensor(Camera)INT#

ADL_P_BGA1744
 REV0.6
 @

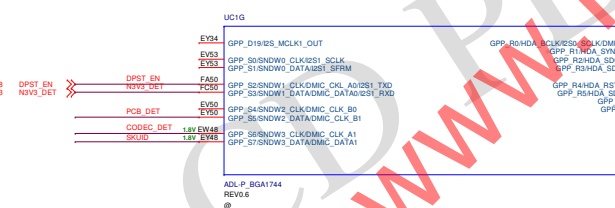


Pin Name	Vendor: VECO/FG Grade C Plastic	Vendor: FG ME Aluminum	Vendor: VECO Grade B ME Aluminum
SPK_DET1	High	Low	High
SPK_DET2	High	High	Low

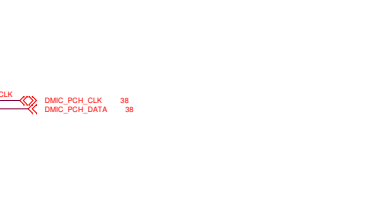
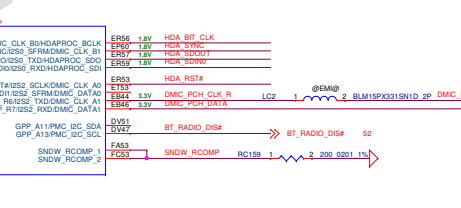


Pin Name	CODEC_DET
Main Realtek Codec	HIGH REALTEK@
2nd Cirrus Codec	LOW CIRRUS@

SKUID	UMA@	LOW
	DIS@	DSC



ADL_P_BGA1744
 REV0.6
 @



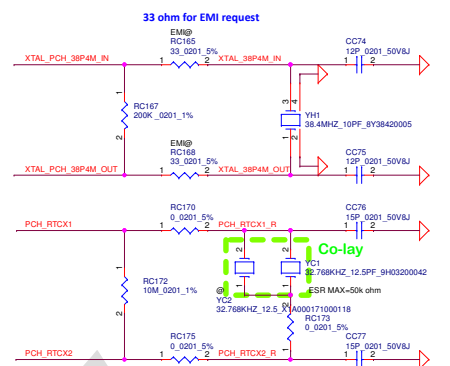
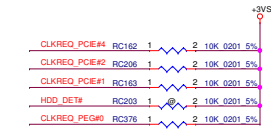
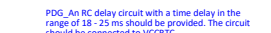
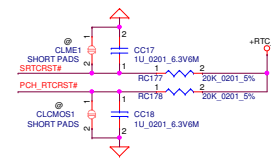
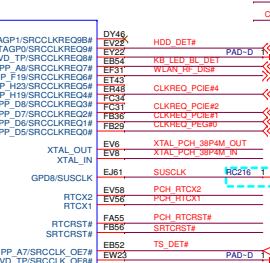
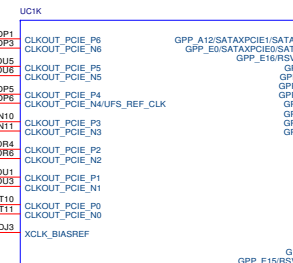
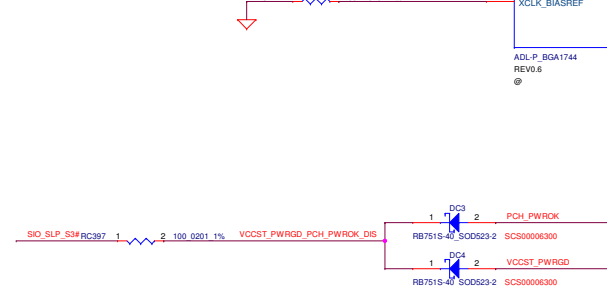
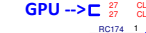
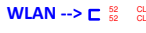
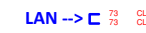
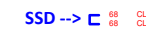
Pin Name	DPST_EN
HIGH	120 Hz Panel
LOW	60 Hz Panel

Pin Name	N3V3_DET
HIGH	N3 non-LAN
LOW	V3 LAN

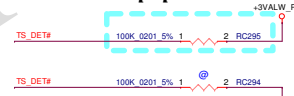
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CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4



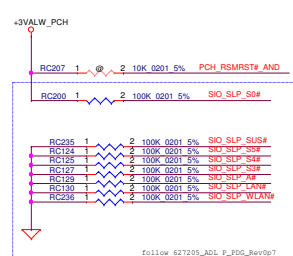
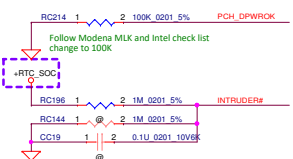
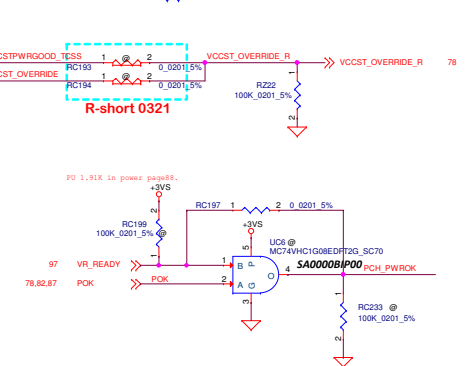
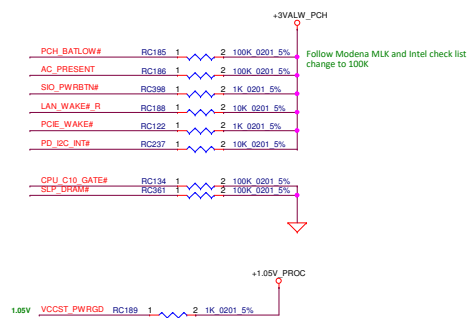
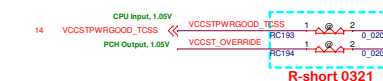
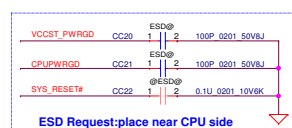
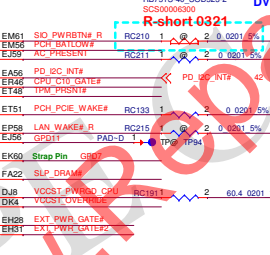
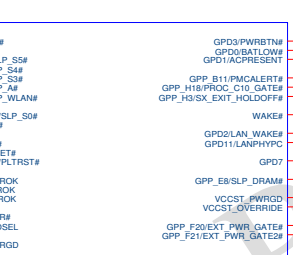
Non-I2CTCH --> RC295 pop



I2CTCH --> *RC294*  *pop*

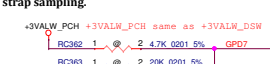
Pin Name	TS_DET#
<i>TOUCH</i>	<i>HIGH</i>
<i>Non TOUCH</i>	<i>LOW</i>

Panel TOUCH DETECT#



Reserved

Weak Internal PD 20k.
This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during

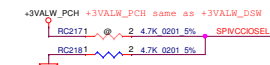


STRAP FOR CPL 1.8V/2.0V CFI

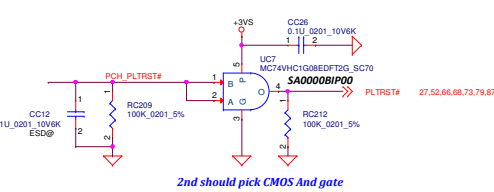
STRAP FOR SPI 1.8V/3.3V SEL
.....

0 = SPI voltage is 3.3V (4.7 k pull-down to GND)

1 = SPI voltage is 1.8V (4.7K pull-up to DSW_PWR)

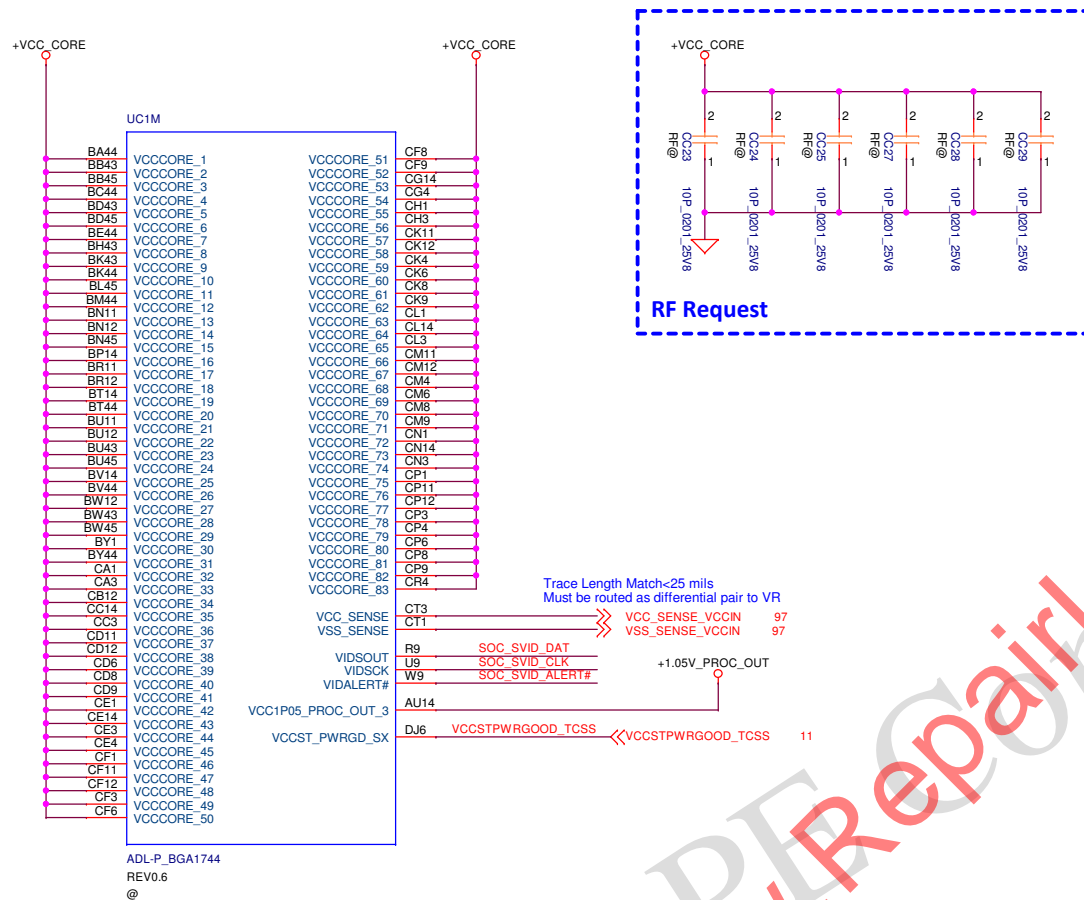


Pin Name	TPM_PRSENT#
<i>LOW</i>	<i>TPM (HW)</i>
<i>HIGH</i>	<i>NTPM (SW)</i>

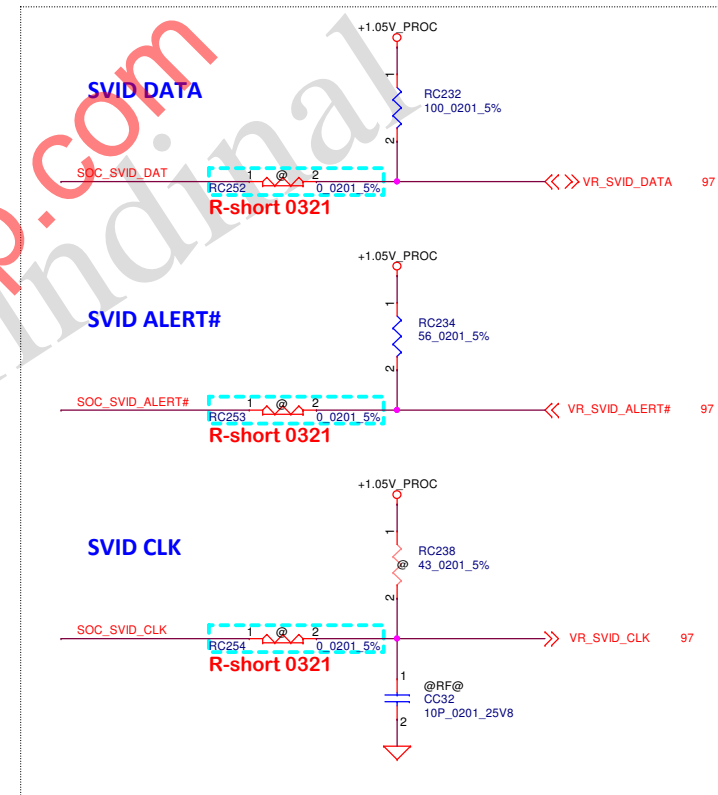
$$TPM/NTPM$$


2nd should pick CMOS And gate

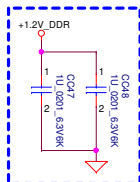
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
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				Size	Document Number	Rev	0.1
				LA-L947P			
Date:		Tuesday, March 22, 2022		Sheet	11 of 121		



1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
 2. Route the Alert signal between the Clock and the Data signals.
- CAD Note: Place the PU resistors close to CPU



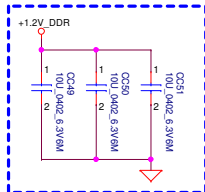
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/10/01	Deciphered Date	2018/10/01	Title	P014 - ADL-P(9/13)CPU PWR,SVID
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					LA-L947P
				Date	Tuesday, March 22, 2022
				Sheet	14 of 121



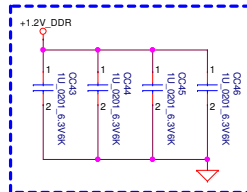
Primary side Cap
2 x 1uF 0402

Secondary Side Cap
2x placeholder
4x 1uF 0402
3x 10uF 0402

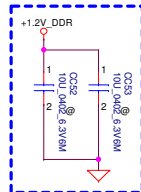
Primary side Caps



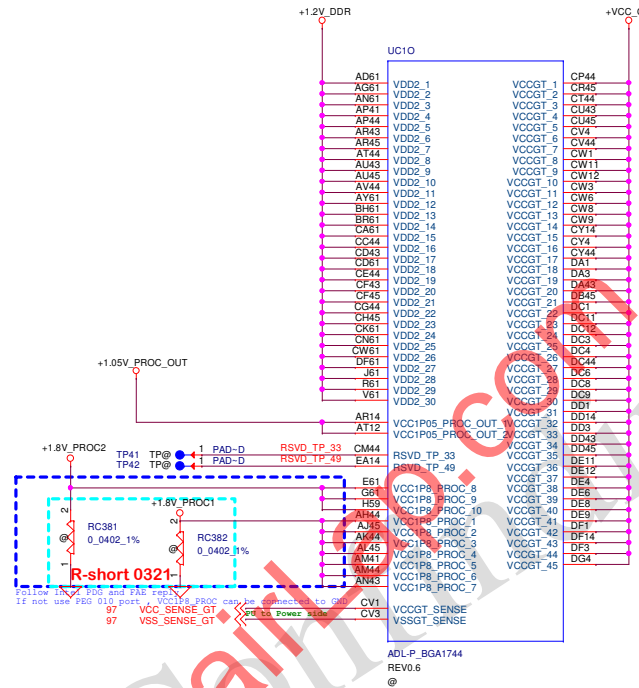
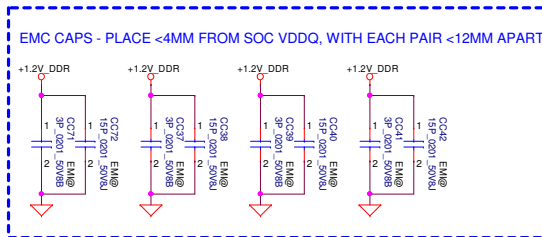
Secondary side Caps



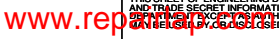
Secondary side Caps



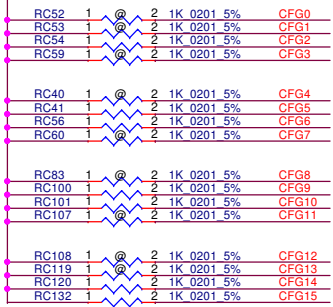
Secondary side Caps Placeholder



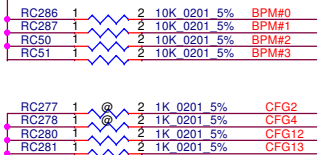
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/10/01	Deciphered Date	2018/10/01	Title	P015 - ADL-P(10/13)CPU PWR
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				Date	LA-1947P
				Sheet	15 of 121



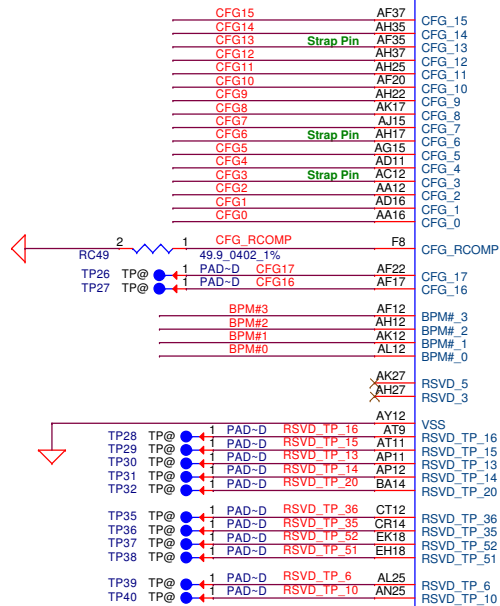
+VCC_CFG_PU_OUT



+VCC_CFG_PU_OUT

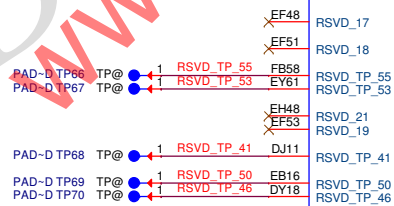


UC1U

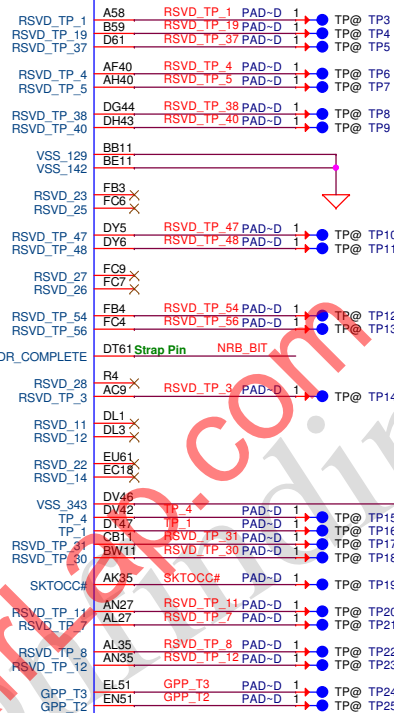


ADL-P_BGA1744
REV0.6
@

UC1T



ADL-P_BGA1744
REV0.6
@



NO REBOOT

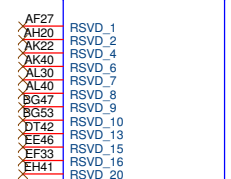
GPP_B18/GSPI0_MOS (Internal 20 K Pull Down)

0 = Disable "No Reboot" mode(Default)

1 = NO REBOOT (This function is useful when running ITP/XDP).



UC1D



ADL-P_BGA1744
REV0.6
@

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2020/10/01				2018/10/01				Title			
P018 - ADL-P(13/13)RSVD				Size				Document Number			
LA-L947P				Rev				0.1			
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18				of				121			

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				Date:	Tuesday, December 14, 2021	Sheet 20 of 121

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					LA-L947P	0.1
				Date:	Tuesday, December 14, 2021	Sheet 21 of 121

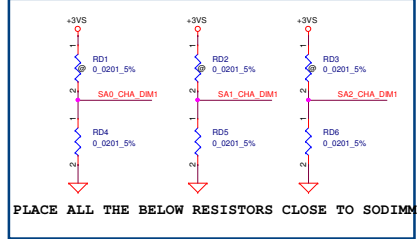
Main Function:

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CHANNEL-M0

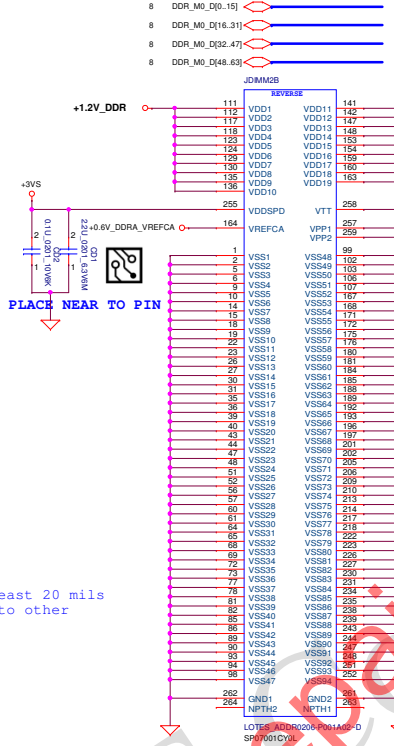
BOT: DIMM1 (JDIMM2 CONN) Non-ECC DIMM



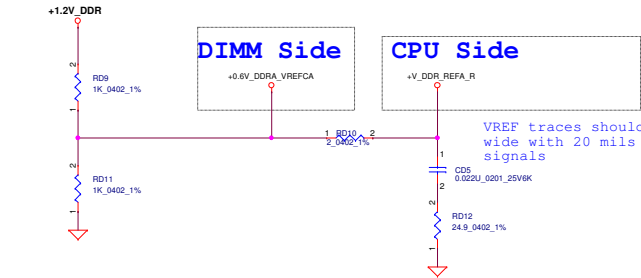
SPD ADDRESS FOR CHANNEL A :

SA0 = 0; SA1 = 0; SA2 = 0.

Non-Interleaved Memory

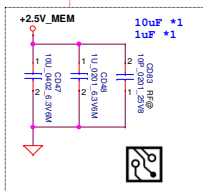


PLACE NEAR TO PIN

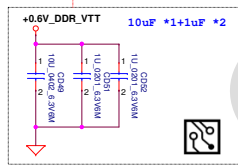


Decoupling Cap_Channel A

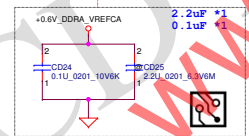
Layout Note: Place near JDIMM2.257,259



Layout Note: Place near JDIMM2.258

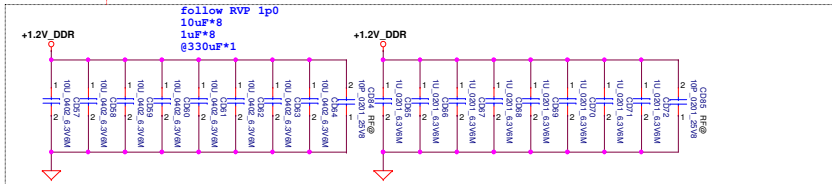


Layout Note: PLACE THE CAP near JDIMM2.164

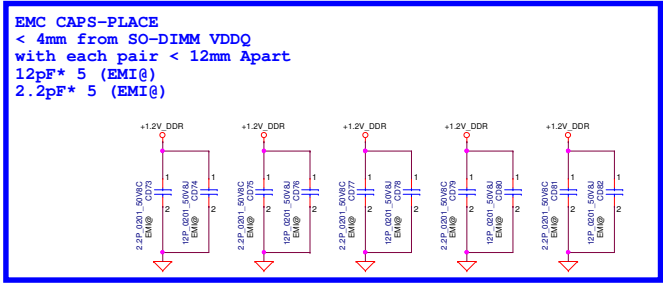
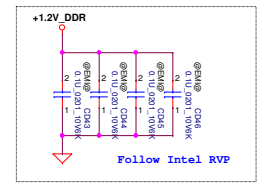
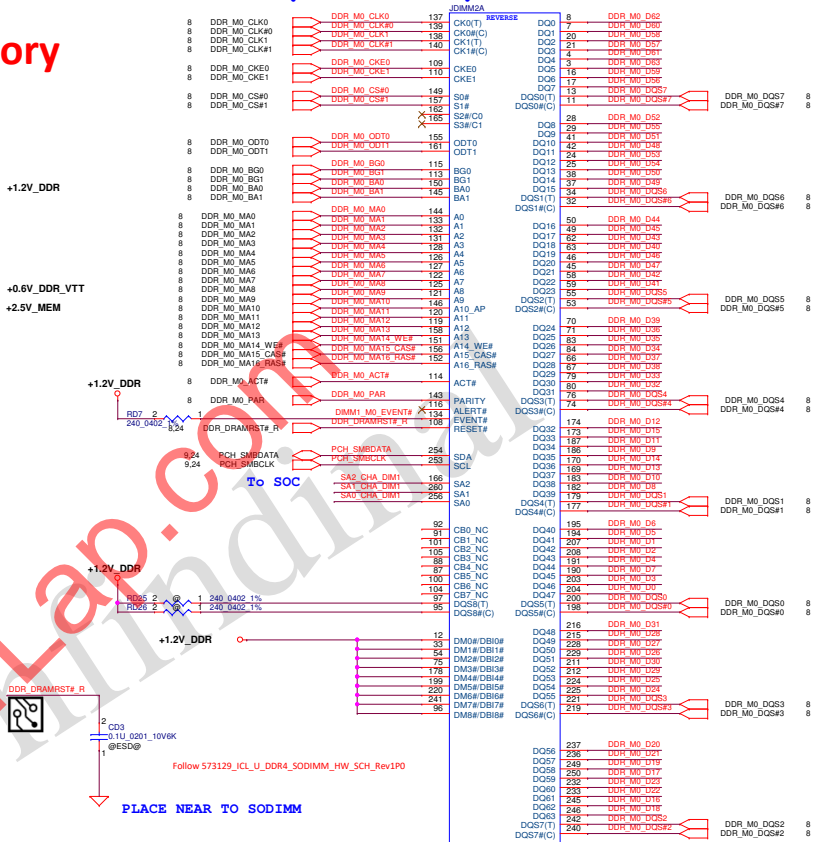


C107 place near JDIMM2

Layout Note: Place near JDIMM2

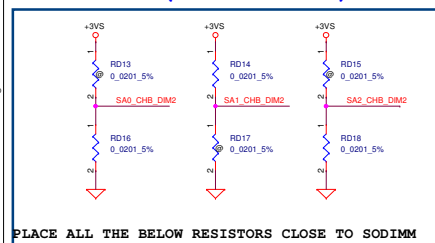


REVERSE TYPE (5.2 mm)

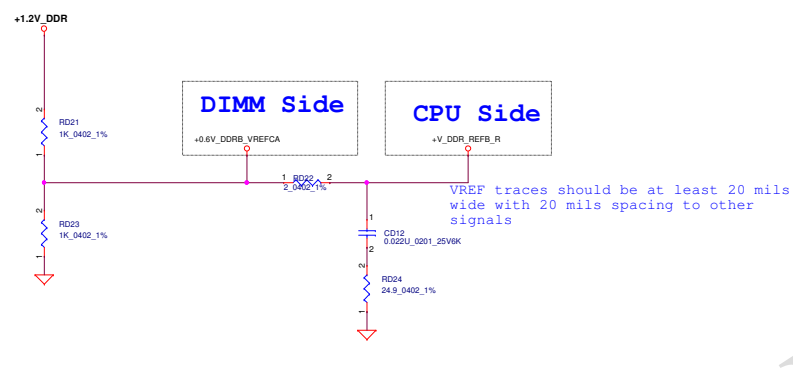


Part Number:SP07001JH00
Part Value:S SOCKET LOTES ADDR0208-P001A 260P DDR4

BOT: DIMM2 (JDIMM1 CONN) Non-ECC DIMM

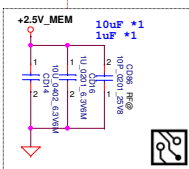


SPD ADDRESS FOR CHANNEL B :

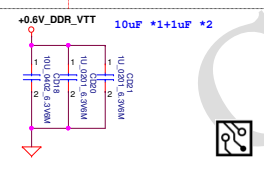
$$SA0 = 0; SA1 = 1; SA2 = 0.$$


Decoupling Cap. Channel B

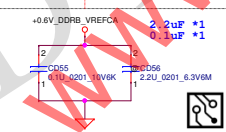
Layout Note:
Place near JDIMM1.257,259



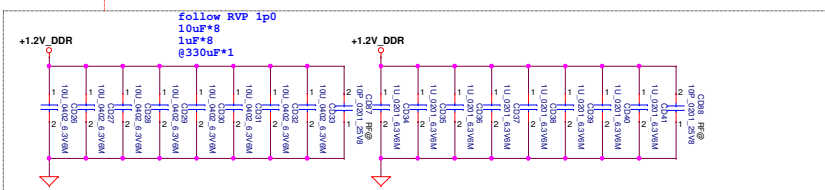
Layout Note:
Place near JDIMM1.258



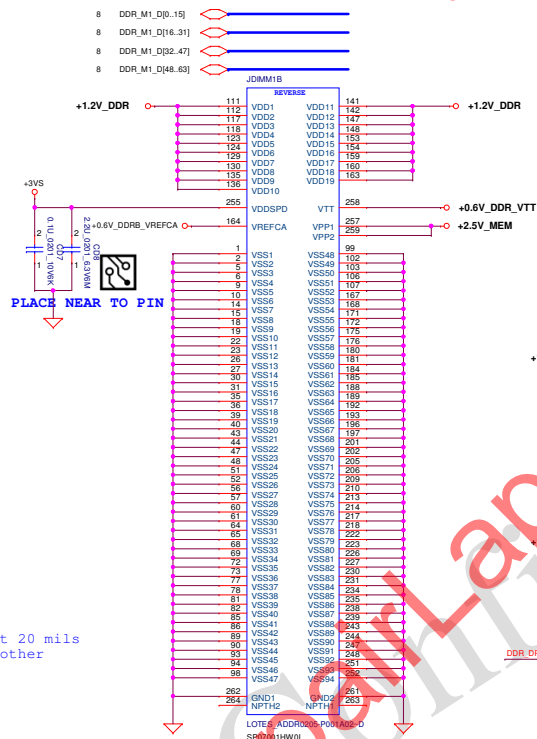
Layout Note:
PLACE THE CAP W
FROM THE JDIMM1



Layout Note:
Place near JDIMM1



Non-Interleaved Memory



PLACE NEAR TO PIN

STD (5.2 mm)



Part Number:SP07001HY00

Part Value: S SOCKET LOTES ADDR0207-P001A 260P DDR4

08/30
Update Table 4-26 for DDR4 SO-DIMM Decoupling Caps
572907 ICL UY PDG Rev0p7 Page.99

Table 4-26. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
DDR4 SODIMM 1DPC	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)
		placeholder	1x 330 μ F (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10 μ F (0603)
		Place on VTT plane close to DIMM	4x 1 μ F (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10 μ F (0603)
		DIMM pin side, 1 per DIMM	2x 1 μ F (0402)
	VDDSPD	Place close to DIMM	2x 0.1 μ F (0402)
Place close to DIMM		2x 2.2 μ F (0402)	

Note:

Note:

1. Total quantity is referring to 2 channels.

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				Sheet	24 of 121

Main Function:

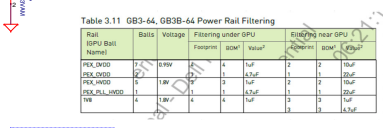
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				Date:	Tuesday, December 14, 2021	Sheet 26 of 121



Under GPU

Near GPU

16 mils

50 mils

Table 3.11 GB3-64, GB3B-64 Power Rail Filtering

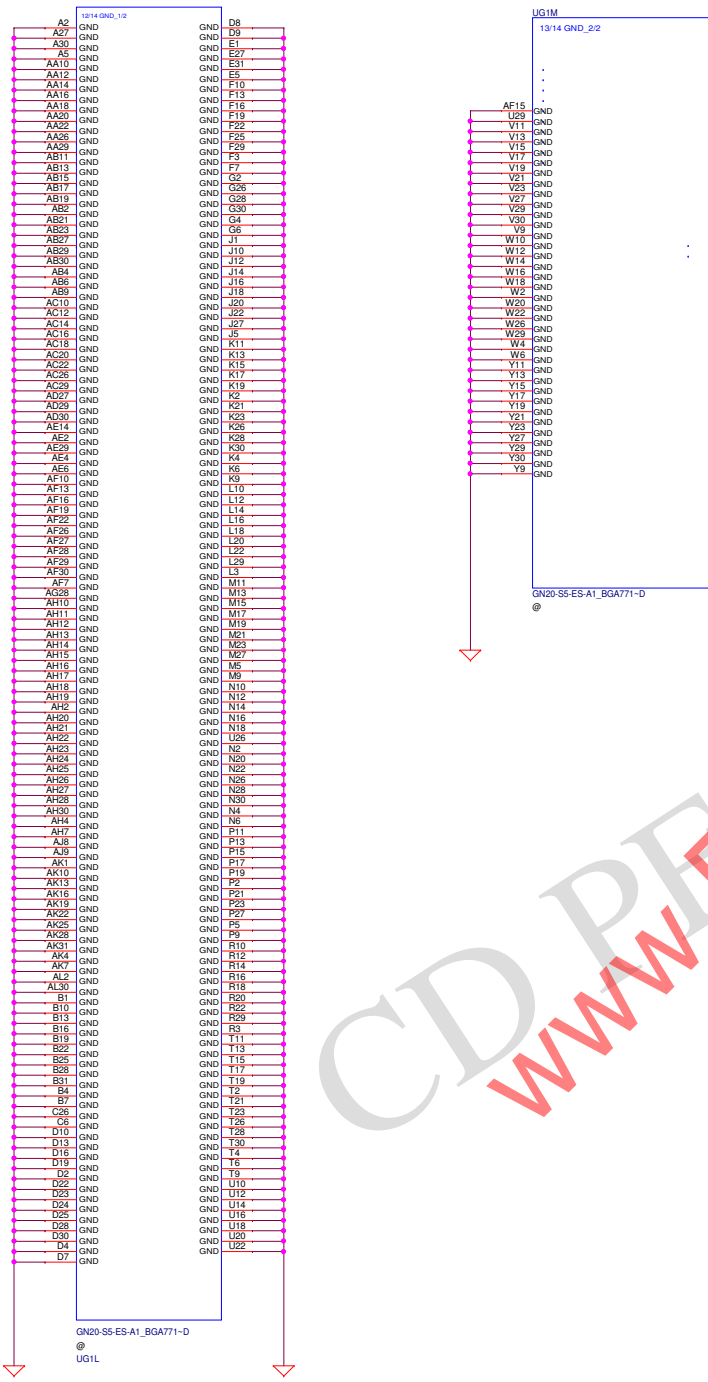
Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU			Filtering near GPU		
			Footprint	BOM	Value	Footprint	BOM	Value
FB_PLLVDD	2	1.8V	2	2	10F (1 per ball)	1	1	300 bead
						1	1	22uF
						2	2	4.7uF

CKE_A

CKE_B

Reset

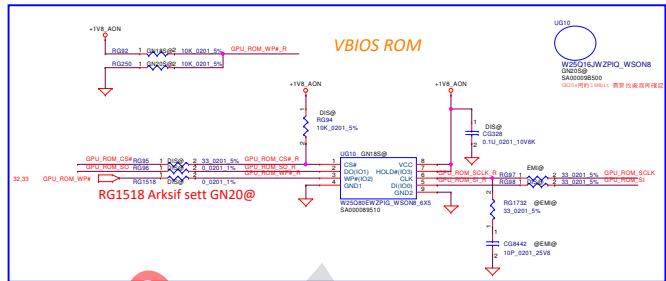
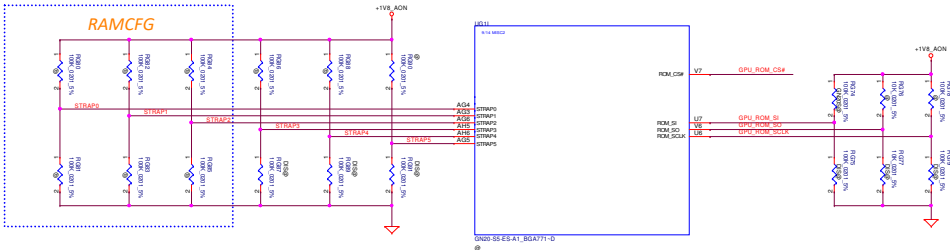
Debug



Main Func = NV - GPU Strap, Rom, Xtal

GDDR6 VRAM	Strap 0	Strap 1	Strap 2
SAMSUNG (D4d)	L	L	L
MICRON (7x7)	H	L	L
HYNIX (Dx2)	L	H	L
HYNIX (Dx5)	H	L	H

FS_OVERT*	ROM_SO	ROM_SI	ROM_SCLK	
GN18-S5	L	L	L	Enable (default)
	L	L	H	Disable
GN20-S5	L	M	L	Enable
	L	L	M	Disable



8G bit GDDR6				
Micron 2GB SKU		Samsung 2GB SKU	Hynix_14Gbps 2GB SKU	Hynix_16Gbps 2GB SKU
R1	R3	R3	R3	R3
UM8 VMGR1@ MT61K256M32JE-14A1.2V SA0000807L R085 VM@ 100K + 5% 0201 SD043100380 R085 VM@ 100K + 5% 0201 SD043100380 R085 VM@ 100K + 5% 0201 SD043100380	UM8 VMGR1@ MT61K256M32JE-14A1.2V SA0000807L R085 VM@ 100K + 5% 0201 SD043100380 R085 VM@ 100K + 5% 0201 SD043100380 R085 VM@ 100K + 5% 0201 SD043100380	UM8 V5GR5@ K4Z80325BC-HC14 1.2V SA0000028L R081 V5@ 100K + 5% 0201 SD043100380 R085 V5@ 100K + 5% 0201 SD043100380 R085 V5@ 100K + 5% 0201 SD043100380	UM8 VH_14_RGR5@ H56C8H24AIR-S2C SA0000028L R081 VH_14@ 100K + 5% 0201 SD043100380 R082 VH_14@ 100K + 5% 0201 SD043100380 R085 VH_14@ 100K + 5% 0201 SD043100380	UM8 VH_16_RGR5@ H56C8H24AIR-S2C SA0000028L R081 VH_16@ 100K + 5% 0201 SD043100380 R083 VH_16@ 100K + 5% 0201 SD043100380 R084 VH_16@ 100K + 5% 0201 SD043100380

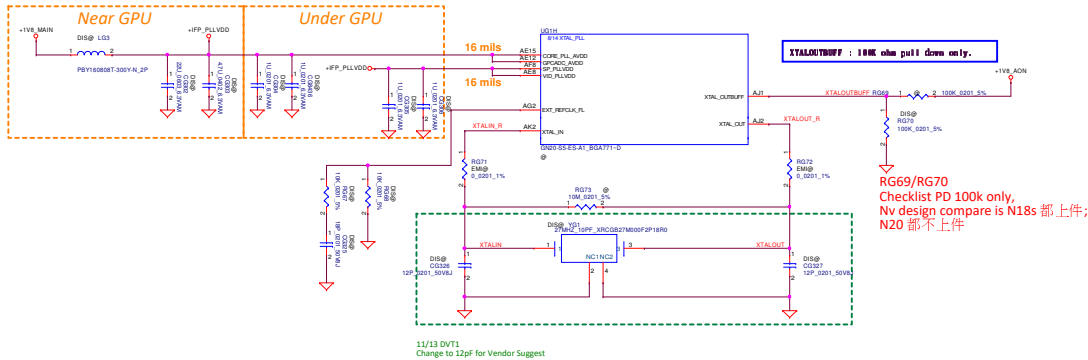
STRAPS	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

- 1.SMB_ALT_ADDR ENABLE
- 0.SMB_ALT_ADDR DISABLE
- 1.DEVID_SEL REBRAND
- 0.DEVID_SEL ORIGINAL
- 1.PCIE_CFG LOW POWER
- 0.PCIE_CFG HIGH POWER
- 1.VGA_DEVICE ENABLE
- 0.VGA_DEVICE DISABLE

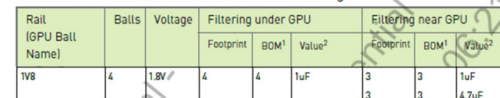
Table 5. GN20-S5 and GN18-S5 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V ¹	Samsung	K4ZAF325BM-HC14	M-die	0x9	14 Gbps	2028	Full	Production candidate	ES or later
			Micron	MT61K512M32KPA-14C	C-die	0x7	14 Gbps	N/A	Full	Post-production candidate	TBD
			Hynix	TBD	TBD	0x8	14 Gbps	N/A	Full	Post-production candidate	TBD
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V ¹	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2028	Full	Production candidate	ES or later
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate	Q5 or later
			Hynix	H56G32C5D-0M85	C-die	0x2	16 Gbps	N/A	Full	Production candidate	PS or later

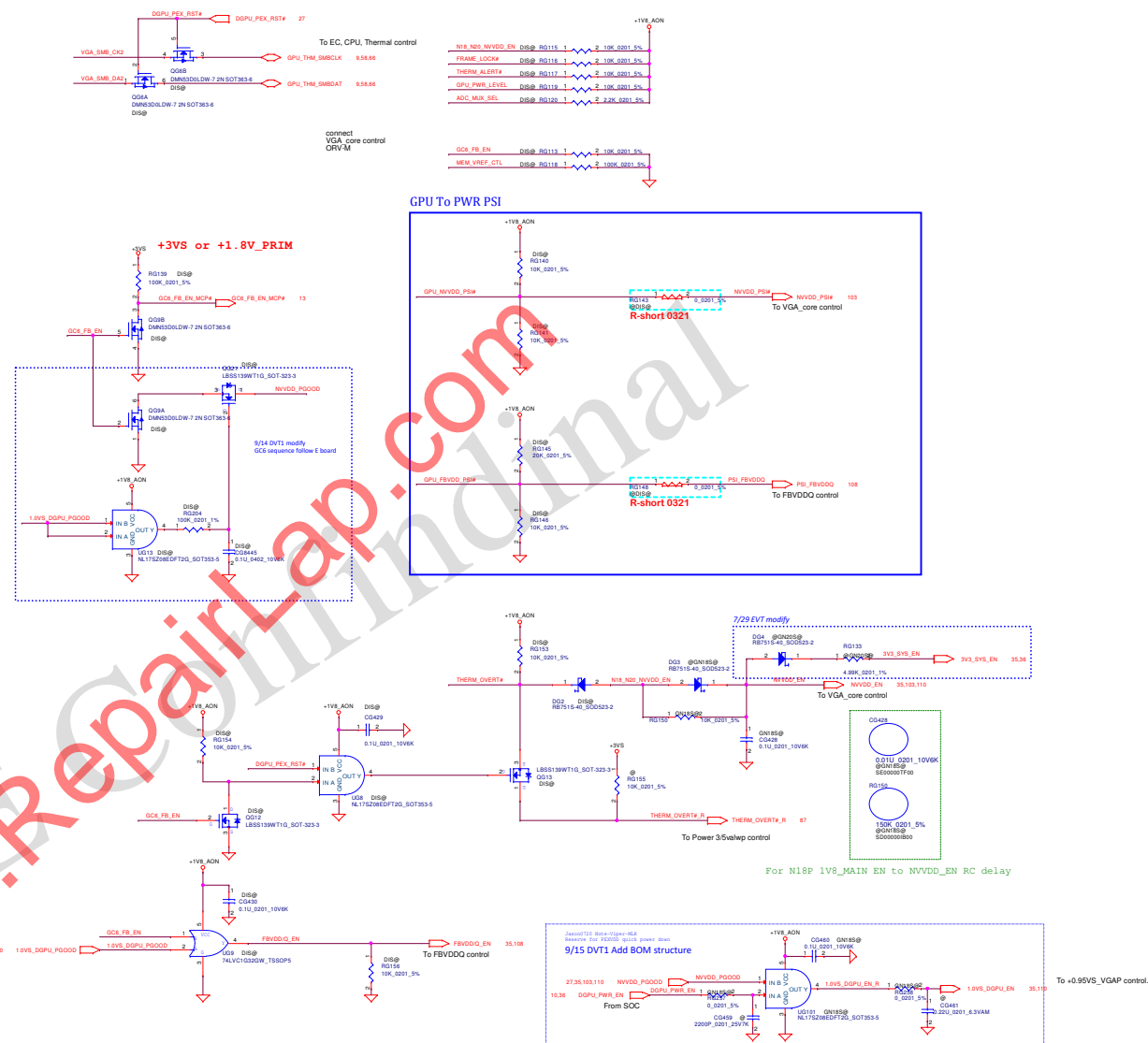
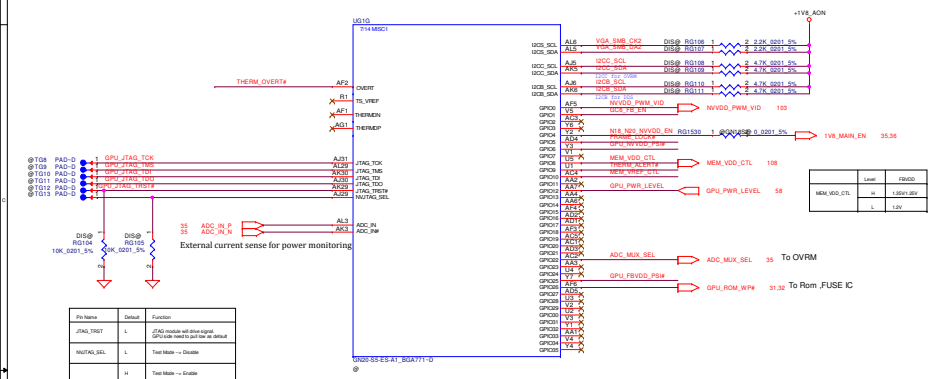
Notes:
* Refer to GN20-S5 and GN18-S5 GeForce GPU Product Spec for memory voltages and clocks.
For GN20-S5 and GN18-S5, the maximum allowable memory case temperature is 105°C.



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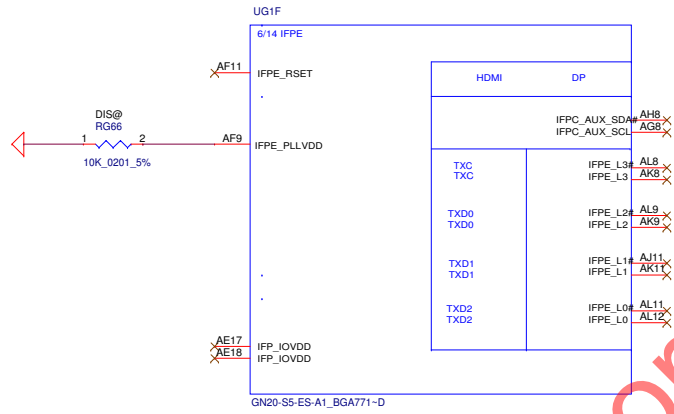
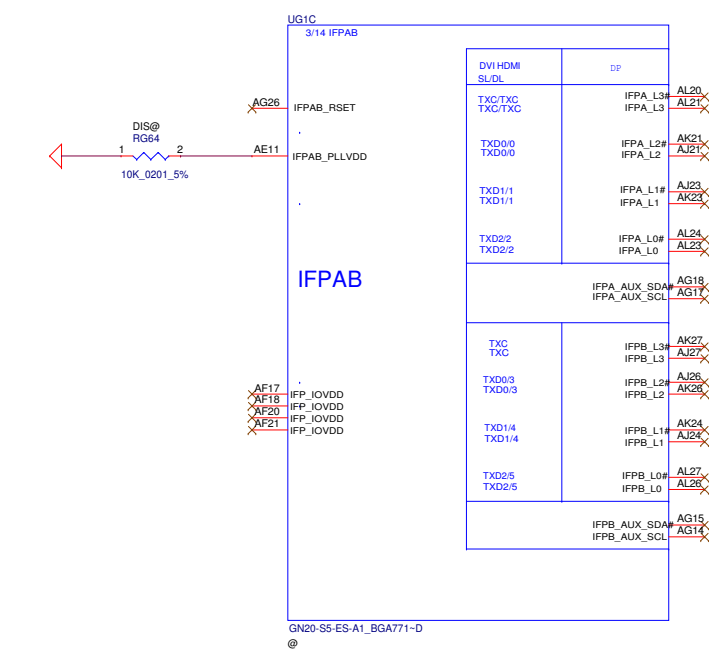


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				Nv(710) MISC L-1947

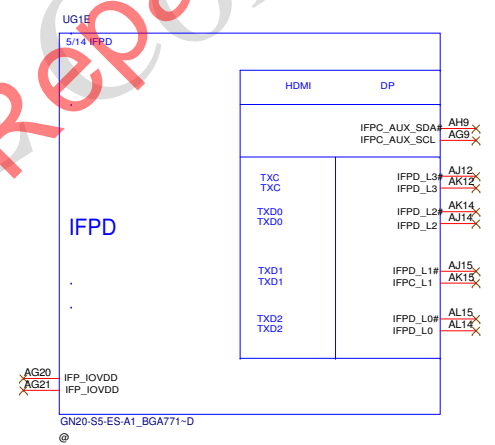
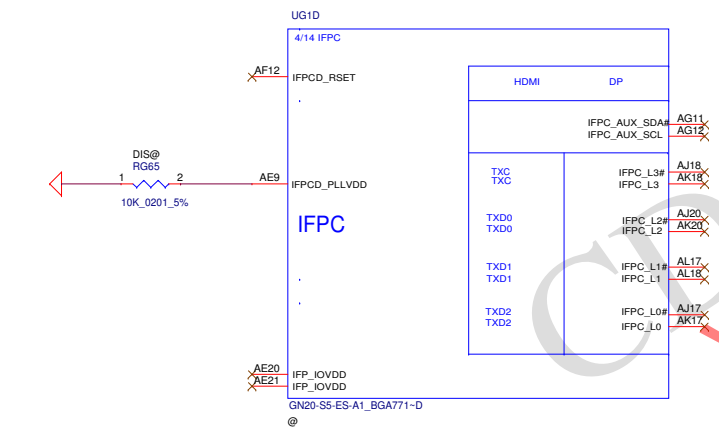
Main Function:Nv - IFP ABCD



7.2 Unused pins

If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET (xy = AB,CD,EF) can be left unconnected and IFPxy_PLLVDD should be 10K PD to GND if neither of IFPx/IFPy is in use. For example, if neither link of the IFPA/IFPB macro is to be used, then IFPAB_PLLVDD must be 10K PD to GND, IFPAB_RSET should be left unconnected, and all signals and references associated with Link A and Link B should also be left unconnected.

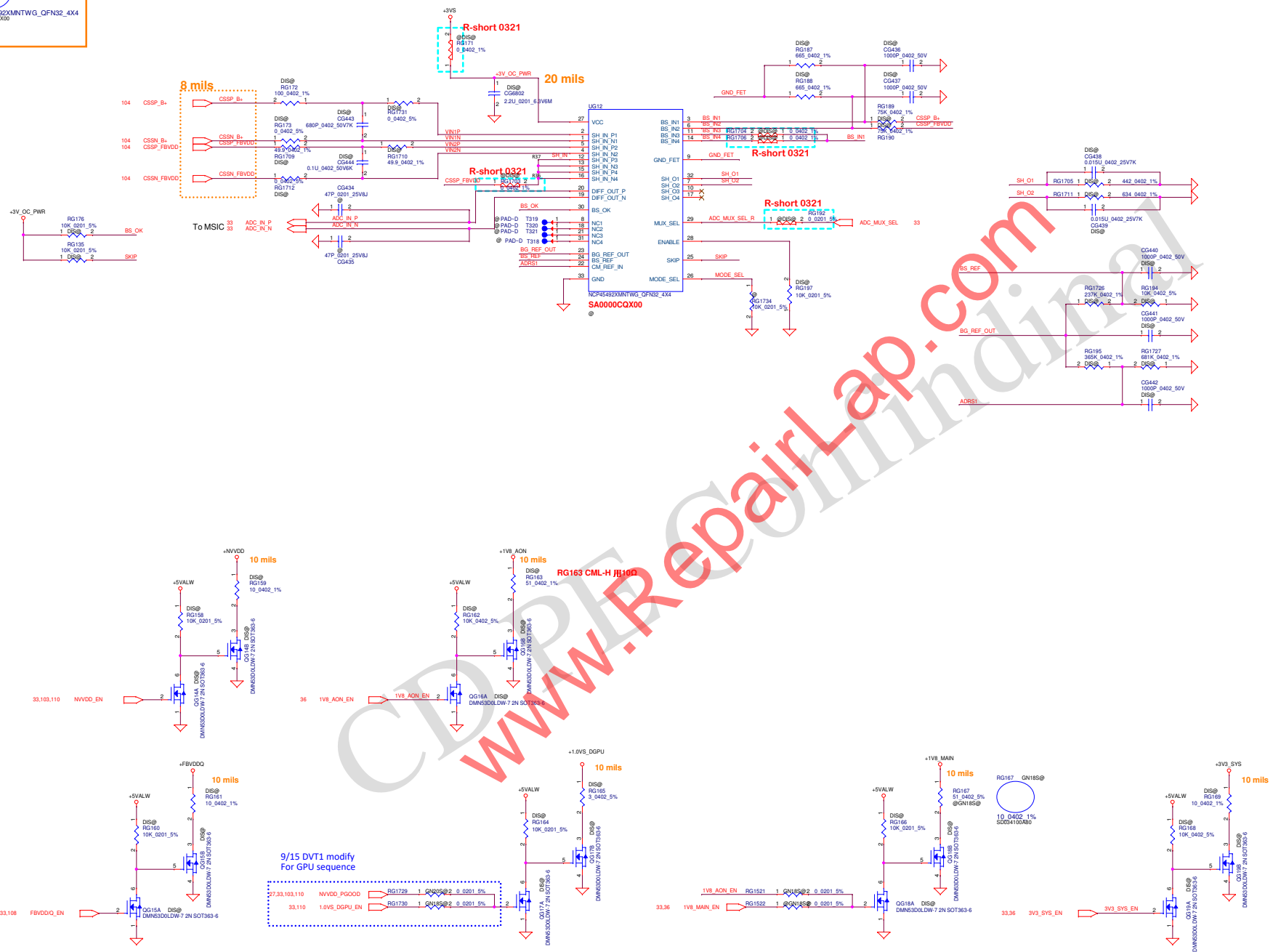
IFP_IOVDD rail can be left unconnected if no IFP link is used. If any IFP is used, all IFP_IOVDD balls must be connected to power rail.



OVRM Gen1 with N18/20s



NCP454520MNTWG_OFN32_4X4
SA0000CQX00
DIS@



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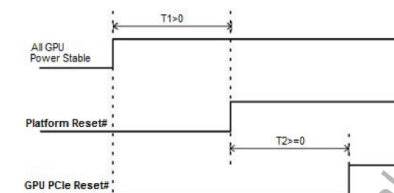


Figure 4.7 GC-OFF 1.0 Entry/Exit Timing Diagram

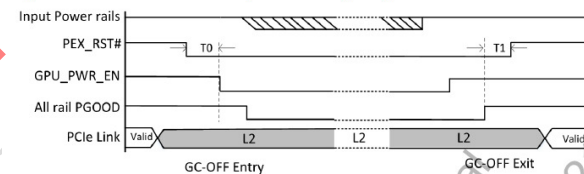
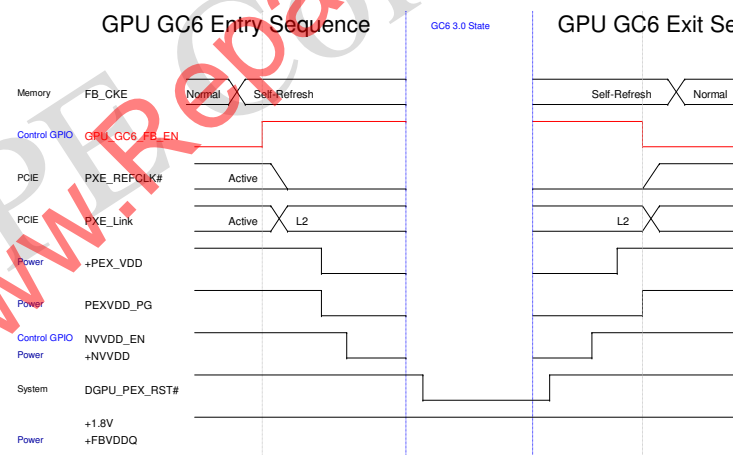
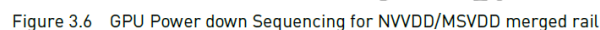


Table 4.4 GC-OFF1.0 Timing Parameters

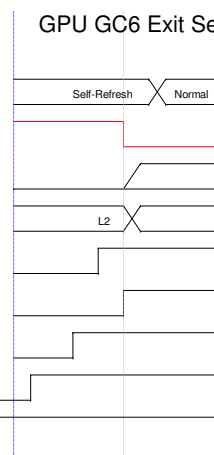
Symbol	Description	Min	Max	Unit
T0	PEX_RST# assertion to GPU_PWR_EN=0	0	5	ms
T1	All GPU power rail up and stable to PEX_RST# deassertion	0.1	5	ms

Figure 3.4 GPU Power Up Sequencing for NVVDD/MSVDD merged rail



The entire entry/exit sequence must complete within 200 ms

GPU GC6 Exit Sequence

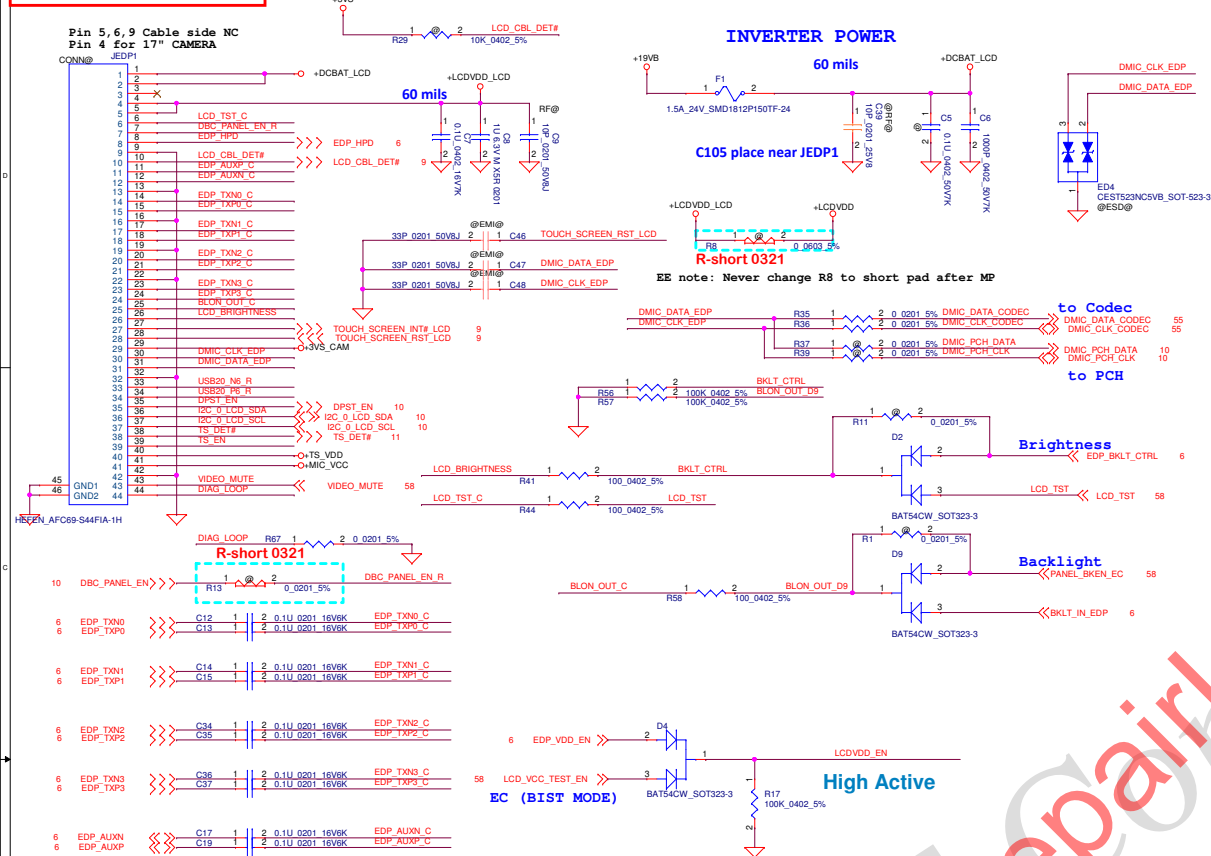


Main Func = GPU DC

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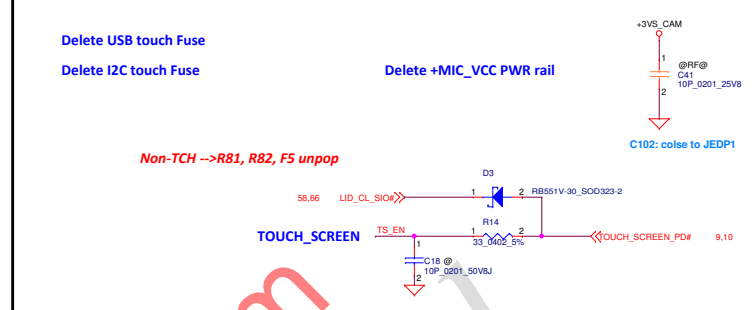
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				Rev	0.1

Main Func = LCD

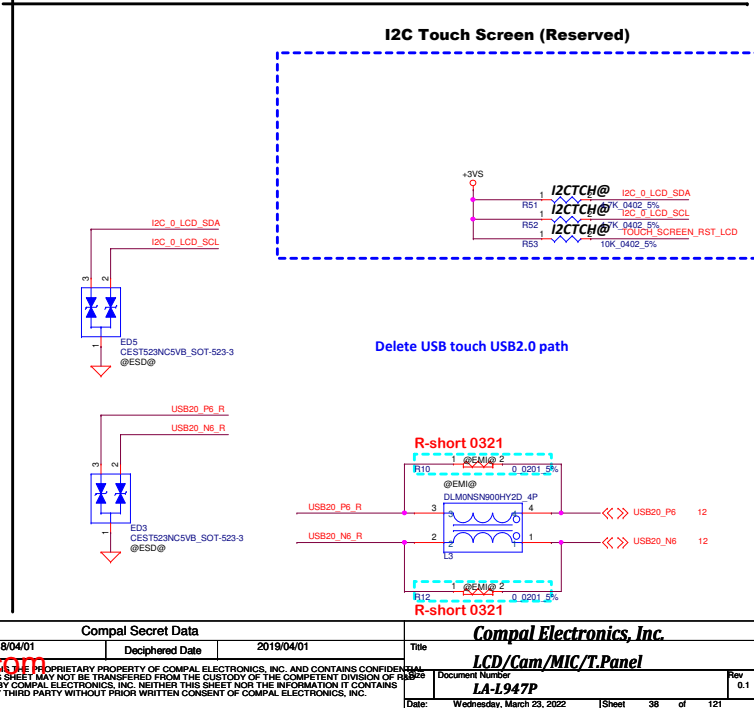
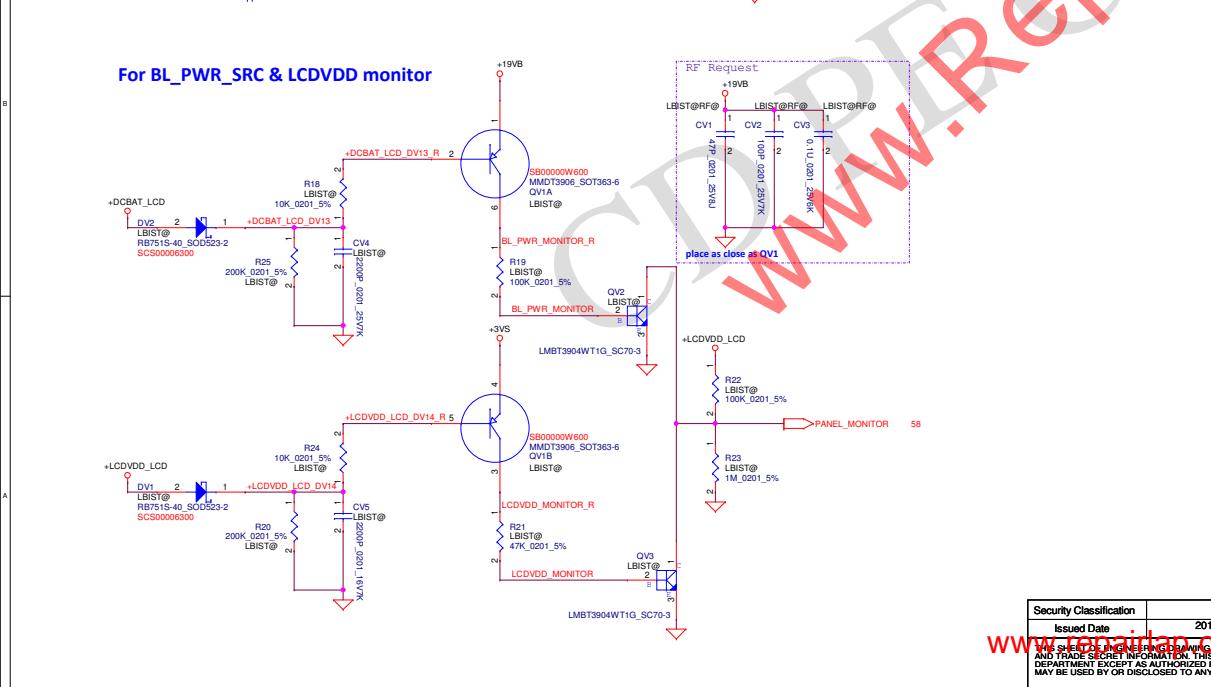
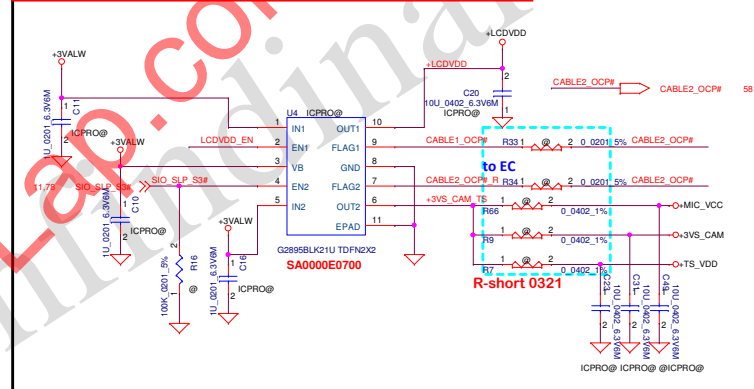


Main Func = CAM&MIC, TS

TCH@ --> Touch Screen
@RF@ --> RF
I2CTCH@ --> I2C Touch Screen
USBTCH@ --> USB Touch Screen



Main Func = Hinge up protection



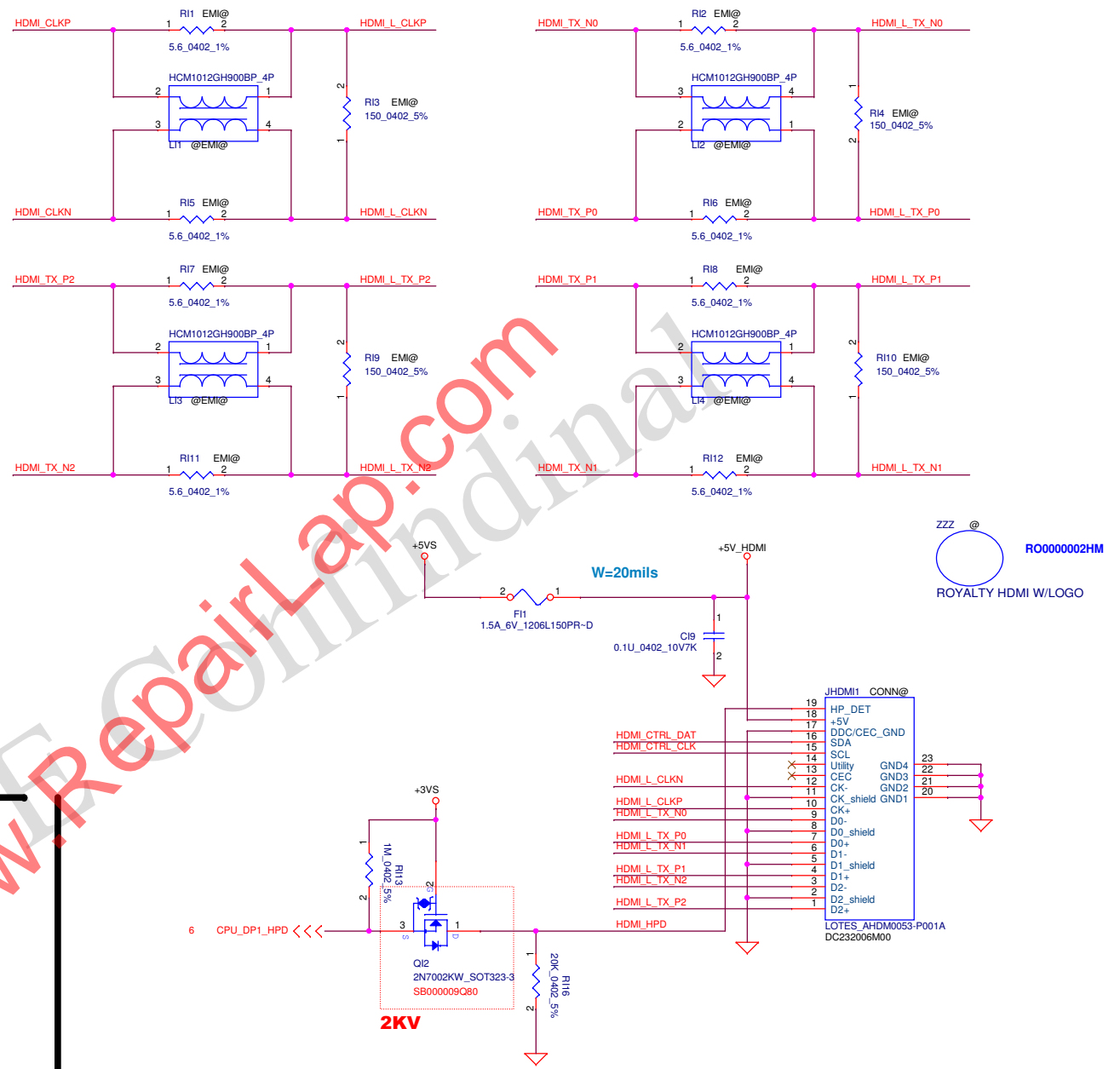
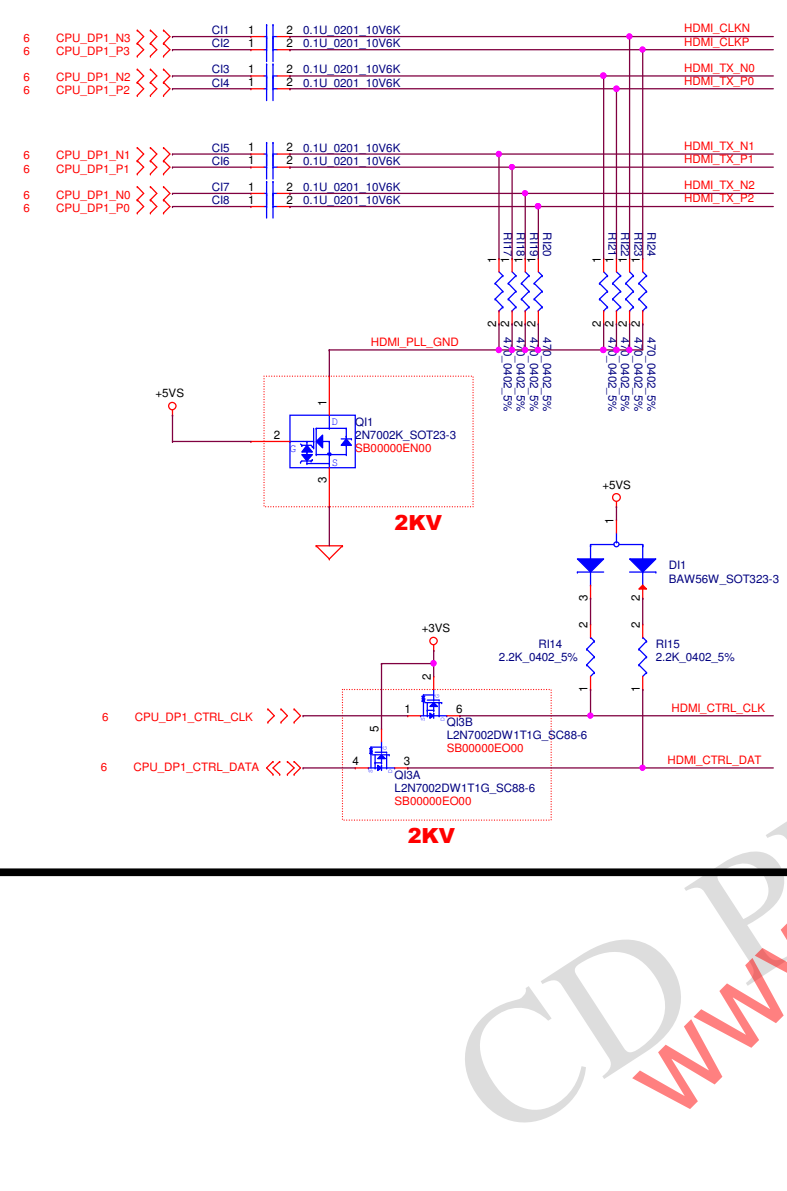
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LA-1947P				Rev 0.1	
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Main Func = HDMI

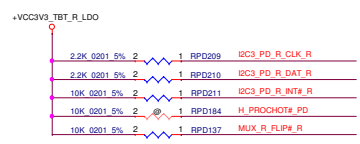
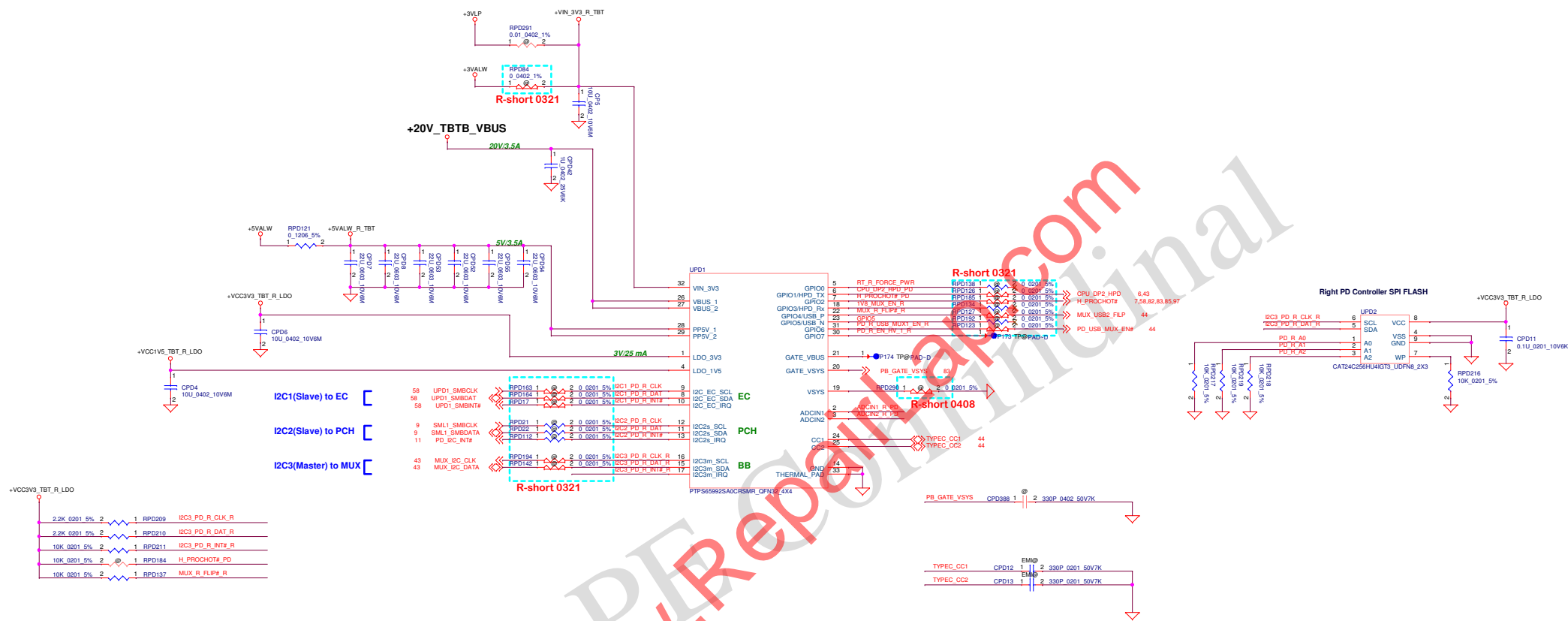


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ADC PD65992 GPIO table			TPS65992D		
GPIO	Pin #	Package Pin Name	TGL w/ Burnside Bridge RT	RKL w/o TBT	RKL w/ TR or MR
0	5	GPIO0	-	-	-
1	6	GPIO1 (HPD_Tx)	RT_EN	HPD_Tx	-
2	7	GPIO2 (PROCHOT#)	PROCHOT#	PROCHOT#	PROCHOT#
3	19	GPIO3	RT_RST	-	TBT_RST
4	26	GPIO4 (USB_P)	DDM_MUX_FLIP*	DDM_MUX_FLIP*	DDM_MUX_FLIP*
5	27	GPIO5 (USB_N)	DDM_MUX_EN*	DDM_MUX_EN*	DDM_MUX_EN*
6	37	GPIO6	USB2_MUX_EN*	USB2_MUX_EN*	USB2_MUX_EN*
7	36	GPIO7	-	-	-

DIV = R2/(R1+R2)
ADCIN1 = 2 (0.09)
ADCIN2 = 0
Port R Address: 0x22

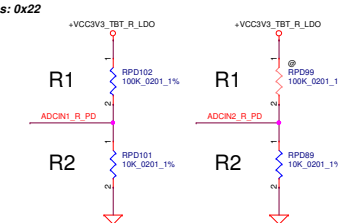
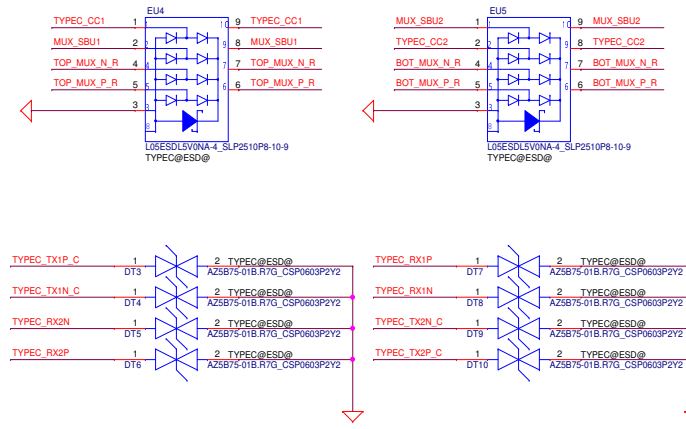
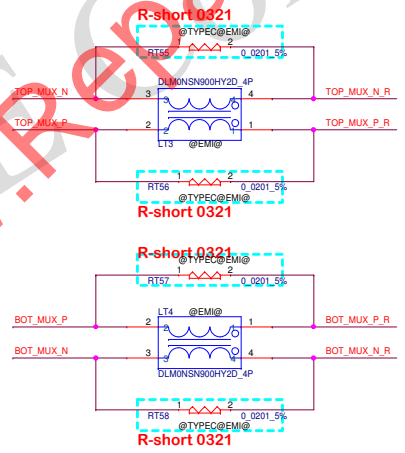
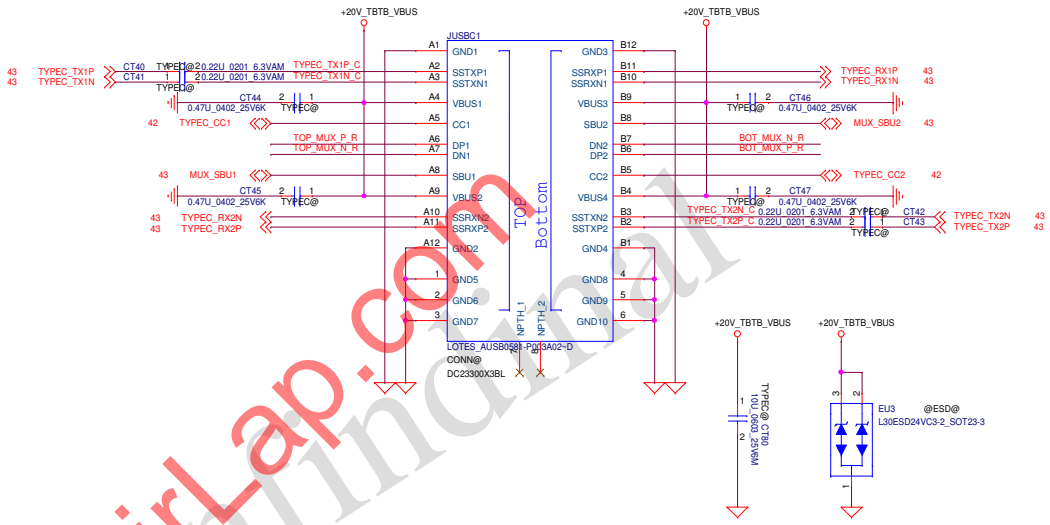
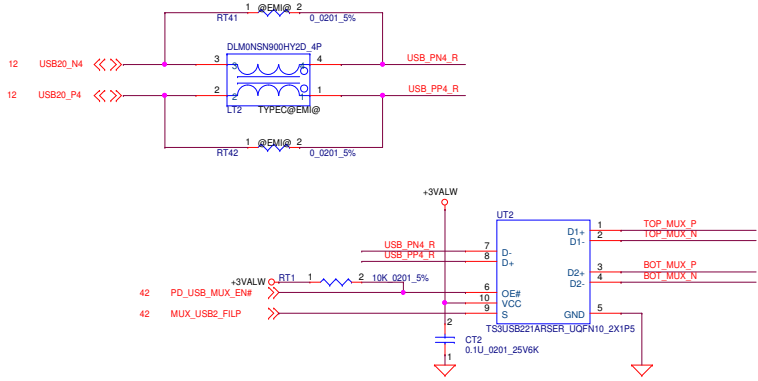


Table 5: I2C Default Slave Address for I2C_EC_SCL/SDA											
I2C address index (decoded from ADCIN1 and ADCIN2)	Port	Slave Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Applicable During BOOT
01	A	0	1	0	0	0	0	0	0	0	Yes
02	A	0	1	0	0	0	0	0	0	1	Yes
03	A	0	1	0	0	0	0	0	1	0	Yes
04	A	0	1	0	0	0	0	0	1	1	Yes

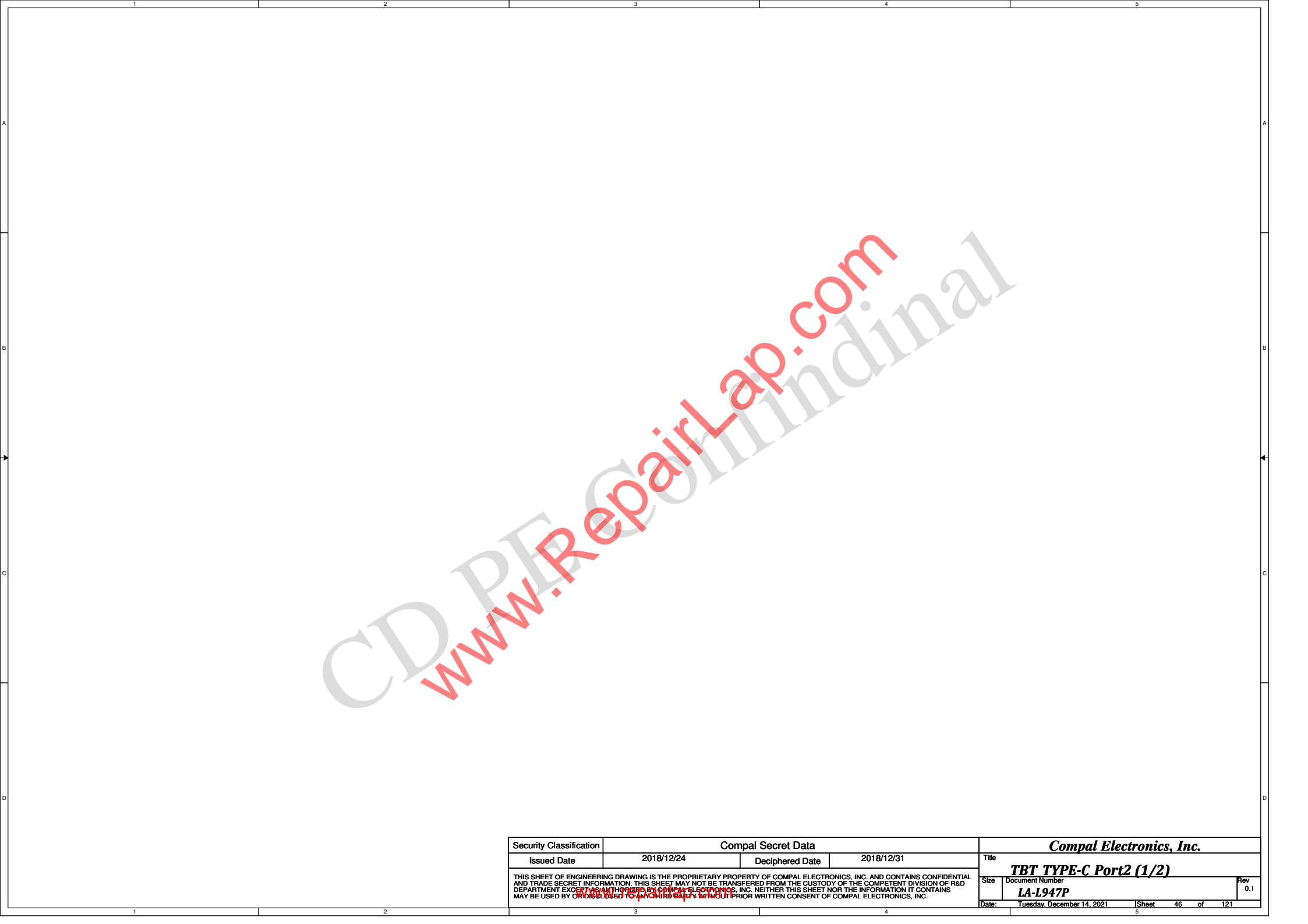
Table 2: Decoding of ADCIN1 and ADCIN2 pins			
BIT	MAX	MIN	ADCIN1/2 decoded value
0	1.023	0.000	0
1	1.023	0.000	1
2	1.023	0.000	2
3	1.023	0.000	3
4	1.023	0.000	4
5	1.023	0.000	5
6	1.023	0.000	6
7	1.023	0.000	7
8	1.023	0.000	8
9	1.023	0.000	9
10	1.023	0.000	10
11	1.023	0.000	11
12	1.023	0.000	12
13	1.023	0.000	13
14	1.023	0.000	14
15	1.023	0.000	15
16	1.023	0.000	16
17	1.023	0.000	17
18	1.023	0.000	18
19	1.023	0.000	19
20	1.023	0.000	20
21	1.023	0.000	21
22	1.023	0.000	22
23	1.023	0.000	23
24	1.023	0.000	24
25	1.023	0.000	25
26	1.023	0.000	26
27	1.023	0.000	27
28	1.023	0.000	28
29	1.023	0.000	29
30	1.023	0.000	30
31	1.023	0.000	31
32	1.023	0.000	32
33	1.023	0.000	33
34	1.023	0.000	34
35	1.023	0.000	35
36	1.023	0.000	36
37	1.023	0.000	37
38	1.023	0.000	38
39	1.023	0.000	39
40	1.023	0.000	40
41	1.023	0.000	41
42	1.023	0.000	42
43	1.023	0.000	43
44	1.023	0.000	44
45	1.023	0.000	45
46	1.023	0.000	46
47	1.023	0.000	47
48	1.023	0.000	48
49	1.023	0.000	49
50	1.023	0.000	50
51	1.023	0.000	51
52	1.023	0.000	52
53	1.023	0.000	53
54	1.023	0.000	54
55	1.023	0.000	55
56	1.023	0.000	56
57	1.023	0.000	57
58	1.023	0.000	58
59	1.023	0.000	59
60	1.023	0.000	60
61	1.023	0.000	61
62	1.023	0.000	62
63	1.023	0.000	63
64	1.023	0.000	64
65	1.023	0.000	65
66	1.023	0.000	66
67	1.023	0.000	67
68	1.023	0.000	68
69	1.023	0.000	69
70	1.023	0.000	70
71	1.023	0.000	71
72	1.023	0.000	72
73	1.023	0.000	73
74	1.023	0.000	74
75	1.023	0.000	75
76	1.023	0.000	76
77	1.023	0.000	77
78	1.023	0.000	78
79	1.023	0.000	79
80	1.023	0.000	80
81	1.023	0.000	81
82	1.023	0.000	82
83	1.023	0.000	83
84	1.023	0.000	84
85	1.023	0.000	85
86	1.023	0.000	86
87	1.023	0.000	87
88	1.023	0.000	88
89	1.023	0.000	89
90	1.023	0.000	90
91	1.023	0.000	91
92	1.023	0.000	92
93	1.023	0.000	93
94	1.023	0.000	94
95	1.023	0.000	95
96	1.023	0.000	96
97	1.023	0.000	97
98	1.023	0.000	98
99	1.023	0.000	99
100	1.023	0.000	100

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				Document Number	
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				0.1	
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				Sheet 45 of 121	



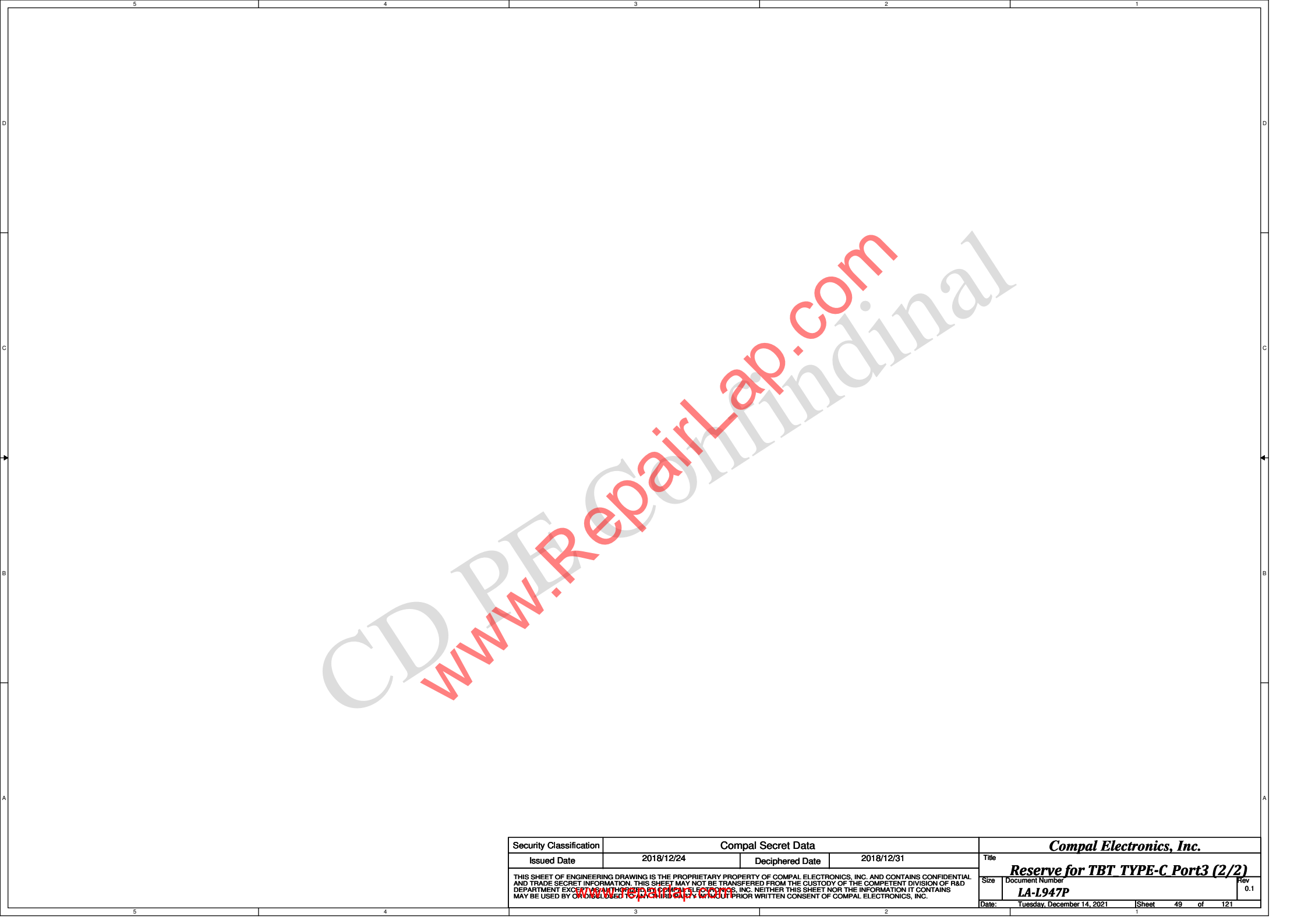
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Issued Date	2018/12/24	Deciphered Date	2018/12/31	Title	TBT TYPE-C Port2 (1/2)
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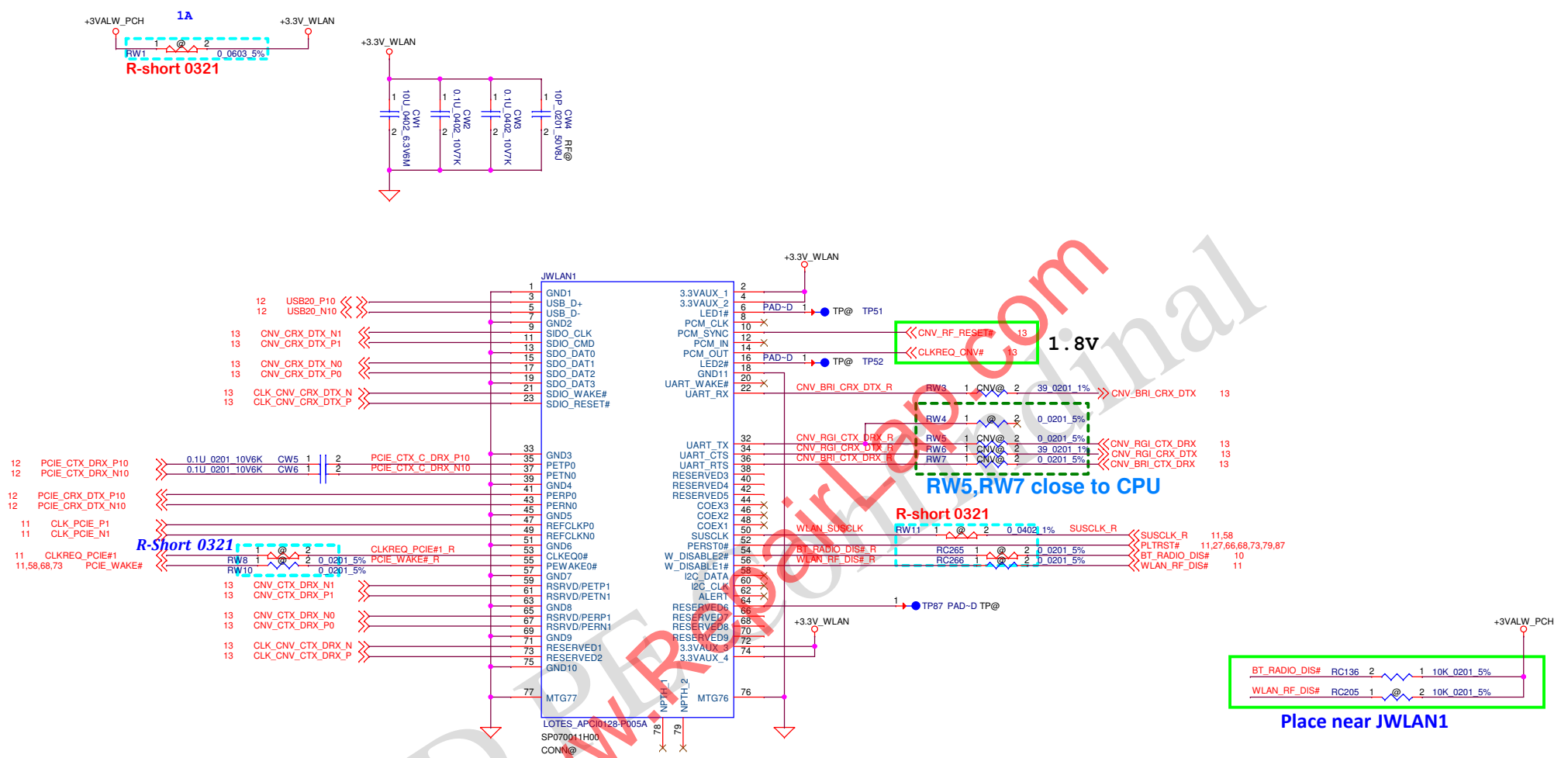
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Main Func = LAN

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Main Func = WLAN E Key CONN



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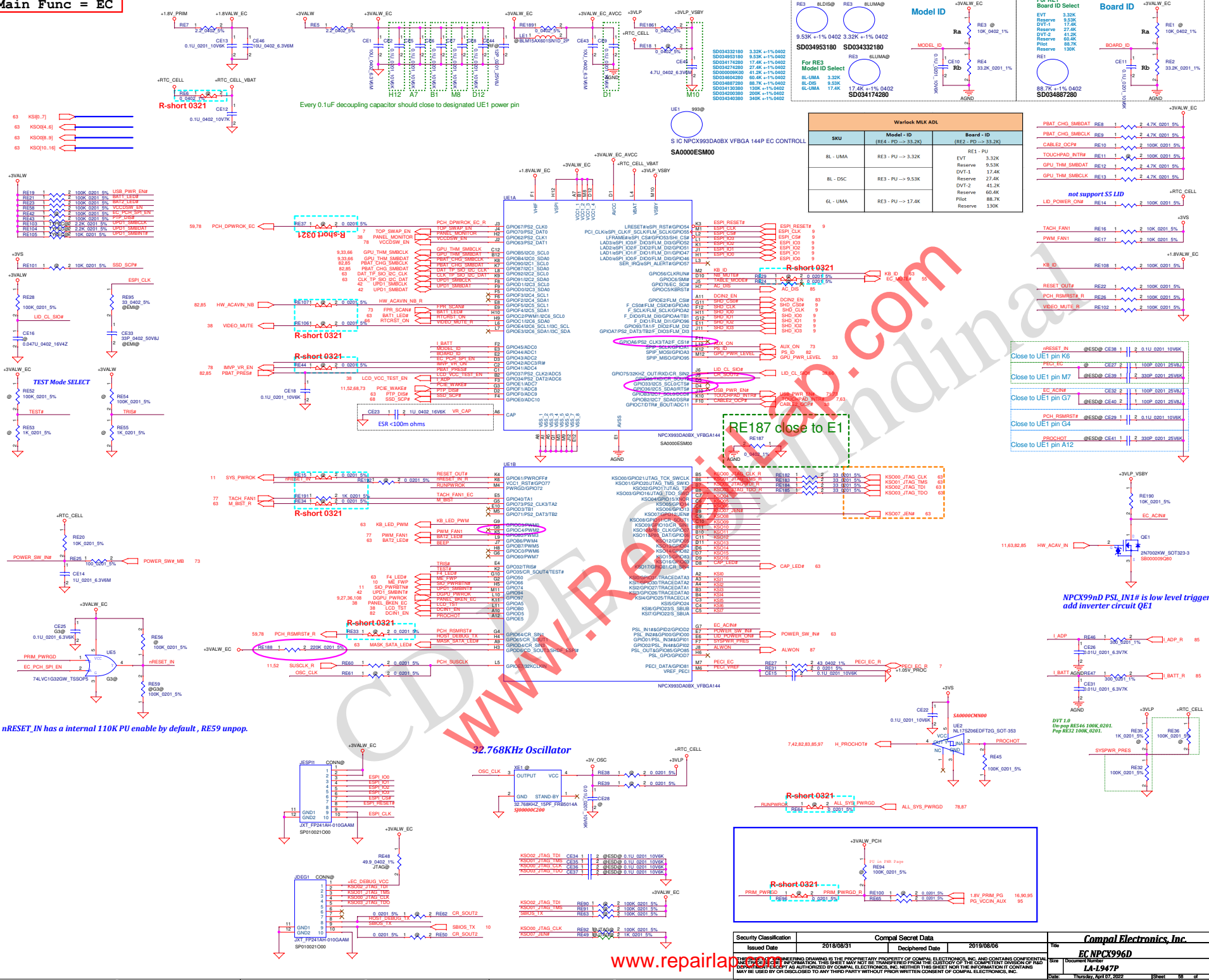
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Main Func = EC

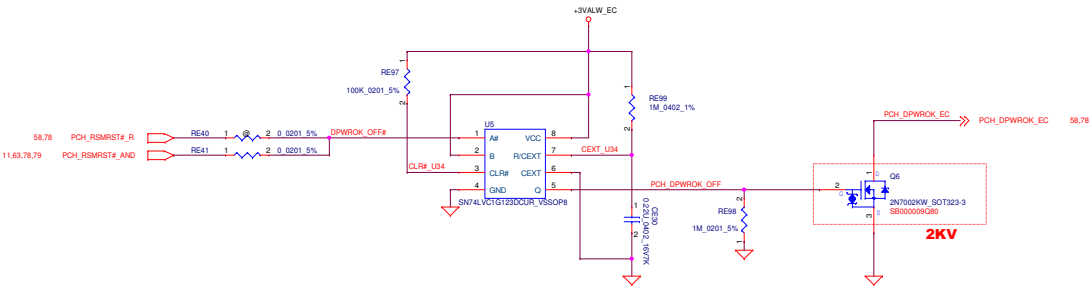


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			LA-1947P	0.1
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Main Function: WDT circuit

FUNCTION TABLE

INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	↑	
H	↓	H	
↑	L	H	



t _{OUT} (2)	Q	C _{int} = 28 pF, R _{int} = 2 kΩ								ns
		225	600	190	220	170	200	150	180	
		100	110	100	110	100	110	100	110	
		1	1.1	1	1.1	1	1.1	1	1.1	
		C _{int} = 0.01 μF, R _{int} = 10 kΩ								μs
		100	110	100	110	100	110	100	110	
		C _{int} = 0.1 μF, R _{int} = 10 kΩ								ms
		1	1.1	1	1.1	1	1.1	1	1.1	

Main Function: S5 LID

Main Function:

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Date: 10/06/2021 09:29:2022 (Sheet 63 of 121)				

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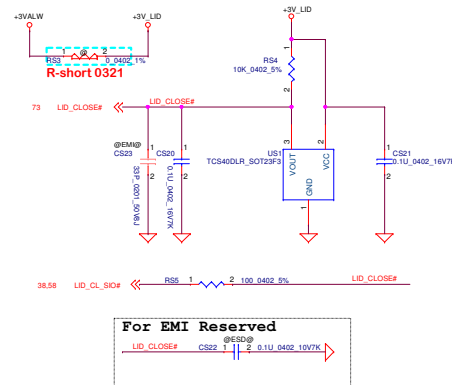
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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title	(RSVD)	
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				Date:	Tuesday, December 14, 2021	Sheet 64 of 121

Main Function:

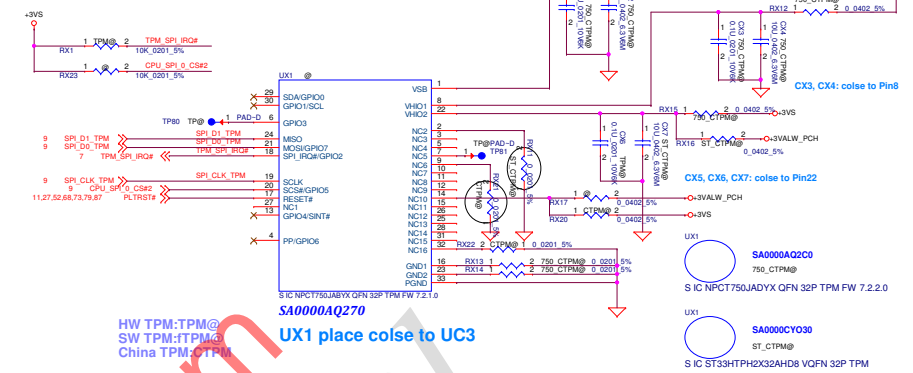
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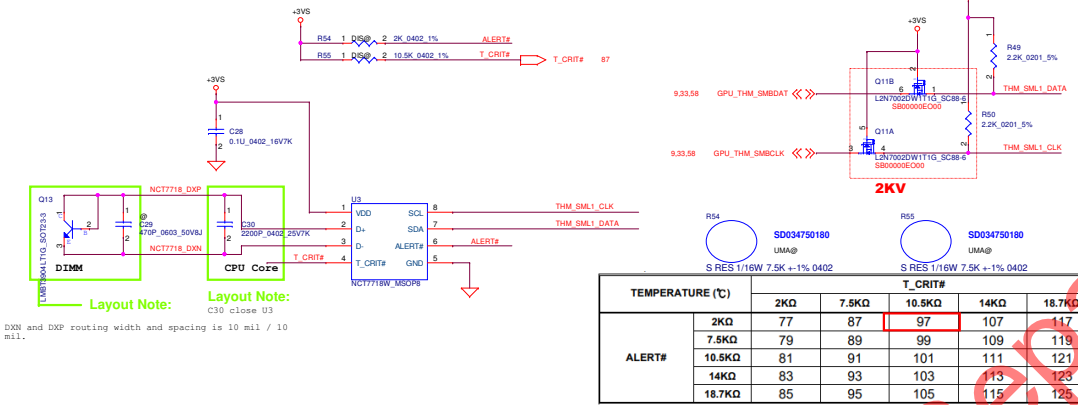
Main Func = Hall Sensor



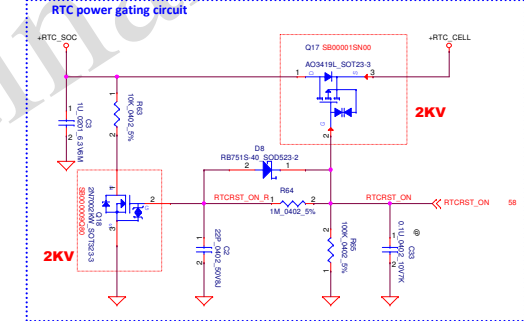
Main Func = TPM



Main Func = Thermal

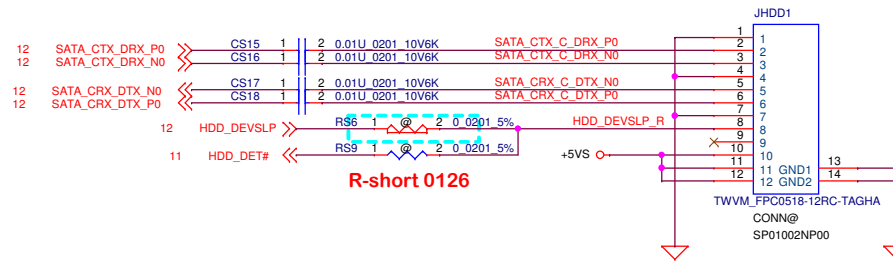
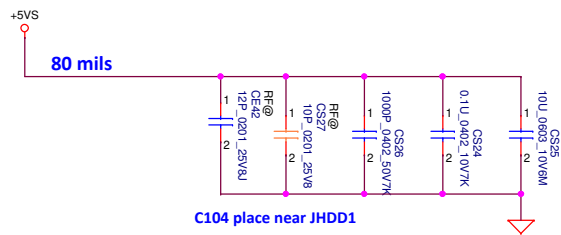


Main Func = RTC



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Main Func = HDD&FFS



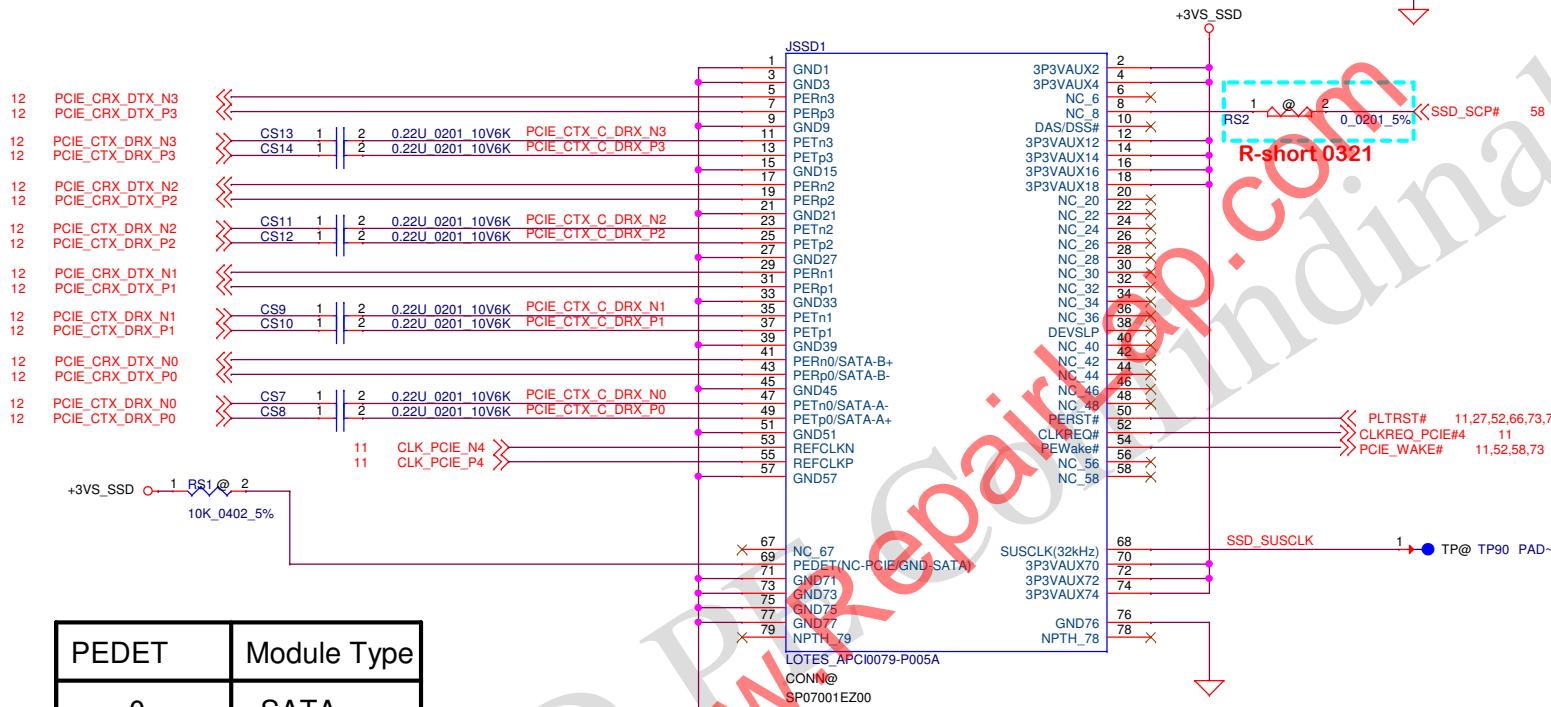
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	8
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	9

Main Func = ODD

Cancel ODD

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NGFF Key M



PEDET	Module Type
0	SATA
1	PCIe

Table 11) Signal Assignments

Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	N/C	N/C
7	PETp3	PCIe TX	8	PLP_IN#(optional)	PLP Control Signal
9	GND	Return current path	10	LED1#	Device Active Signal (Refer to Table 12)
11	PERn3	PCIe Rx	12	3.3V	3.3V source
13	PERp3	PCIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	N/C	N/C
21	GND	Return current path	22	N/C	N/C
23	PERn2	PCIe Rx	24	N/C	N/C
25	PERp2	PCIe Rx	26	N/C	N/C
27	GND	Return current path	28	N/C	N/C
29	PETn1	PCIe TX	30	N/C	N/C
31	PETp1	PCIe TX	32	N/C	N/C
33	GND	Return current path	34	N/C	N/C
35	PERn1	PCIe Rx	36	N/C	N/C
37	PERp1	PCIe Rx	38	N/C	N/C
39	GND	Return current path	40	SMB_CLK (I/O) ²	DNU (Do Not Use)
41	PETn0	PCIe TX	42	SMB_DATA (I/O) ²	DNU (Do Not Use)
43	PETp0	PCIe TX	44	ALERT# (O) ¹	DNU (Do Not Use)
45	GND	Return current path	46	N/C	N/C
47	PERn0	PCIe Rx	48	N/C	N/C
49	PERp0	PCIe Rx	50	PERST#	PCIe Reset
51	GND	Return current path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEVale#	N/C
55	REFCLKP	PCIe Reference Clock	56	Reserved for MFG Data	DNU (Do Not Use)
57	GND	Return current path	58	Reserved for MFG Data	DNU (Do Not Use)
67	N/C	N/C	68	SUSCLK	DNU (Do Not Use)
69	PEDET	N/C	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path	76	3.3V	3.3V source

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Main Func = eMMC

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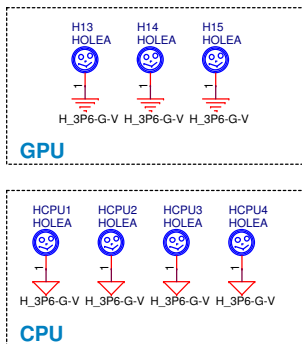
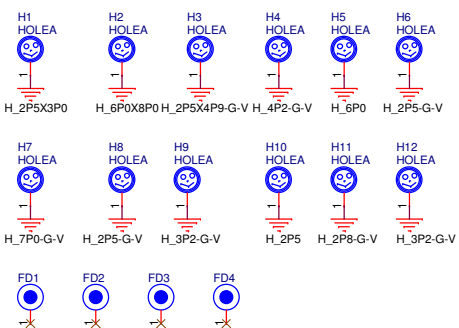
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Main Function:

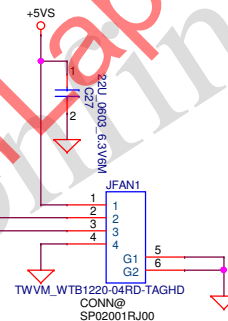
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Screw hole/FD

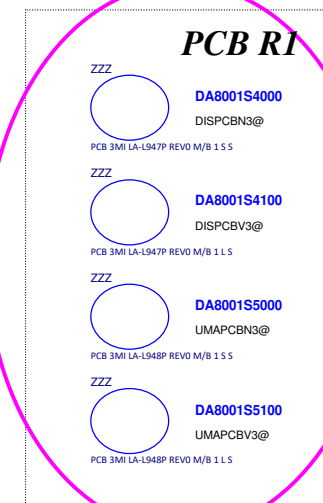


FAN



need to check pin define with Thermal

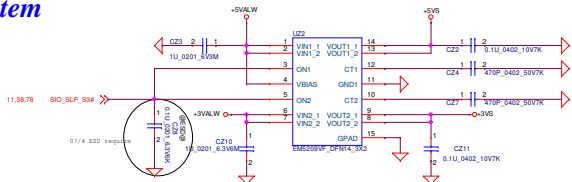
PCB PN



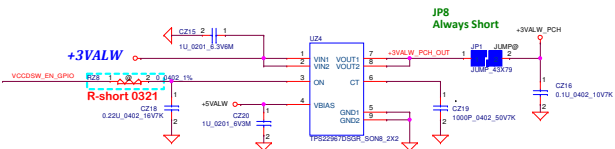
0519 ME update

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Deciphered Date				2019/04/01				PWRBTN/PCB PN//SCREW/FAN			
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								Rev 0.1			

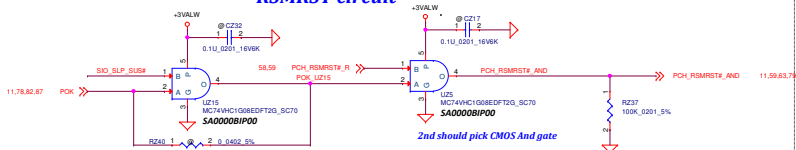
+5VS / +3VS for System



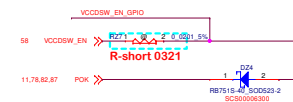
+3VALW TO +3VALW_PCH



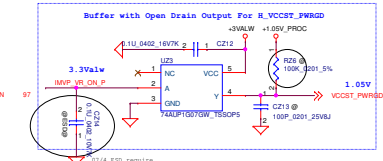
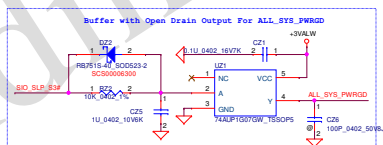
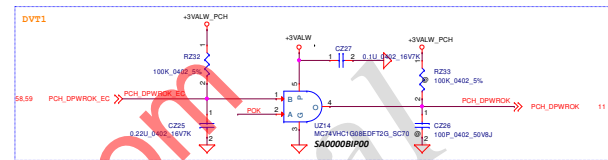
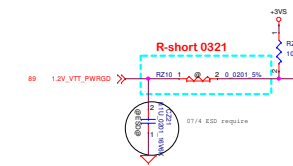
RSMRST circuit



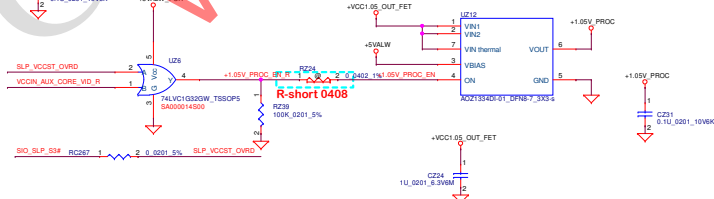
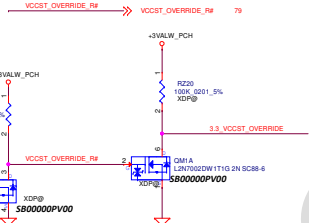
Sequence Logic



IMVP_VR_ON&VCCST_PWRGD



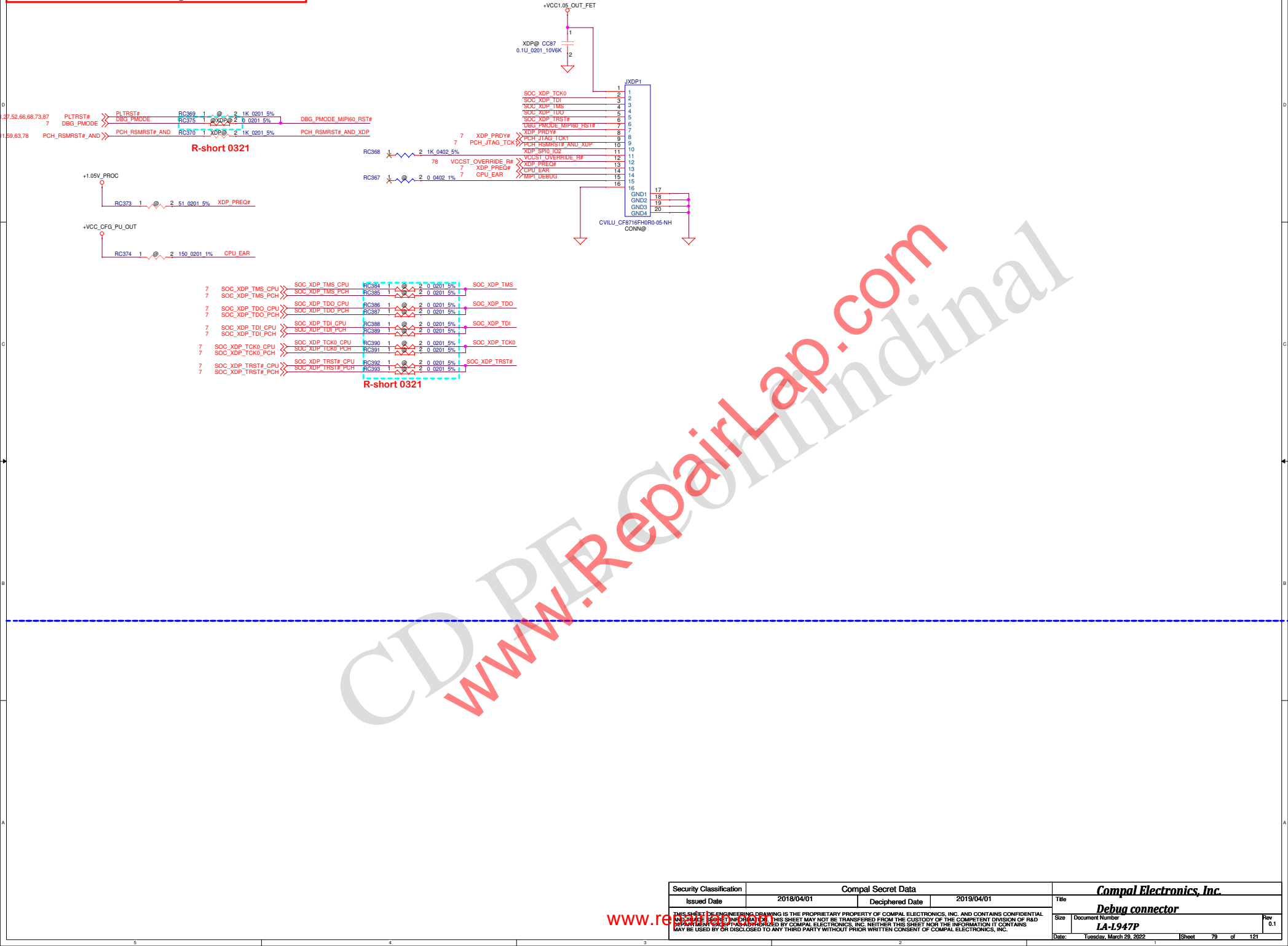
1.05V_PROC



SN74AUP1C FUNCTION TABLE with table

INPUTS		OUTPUT	
A	B	A	B
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L

Main Func = Debug connector



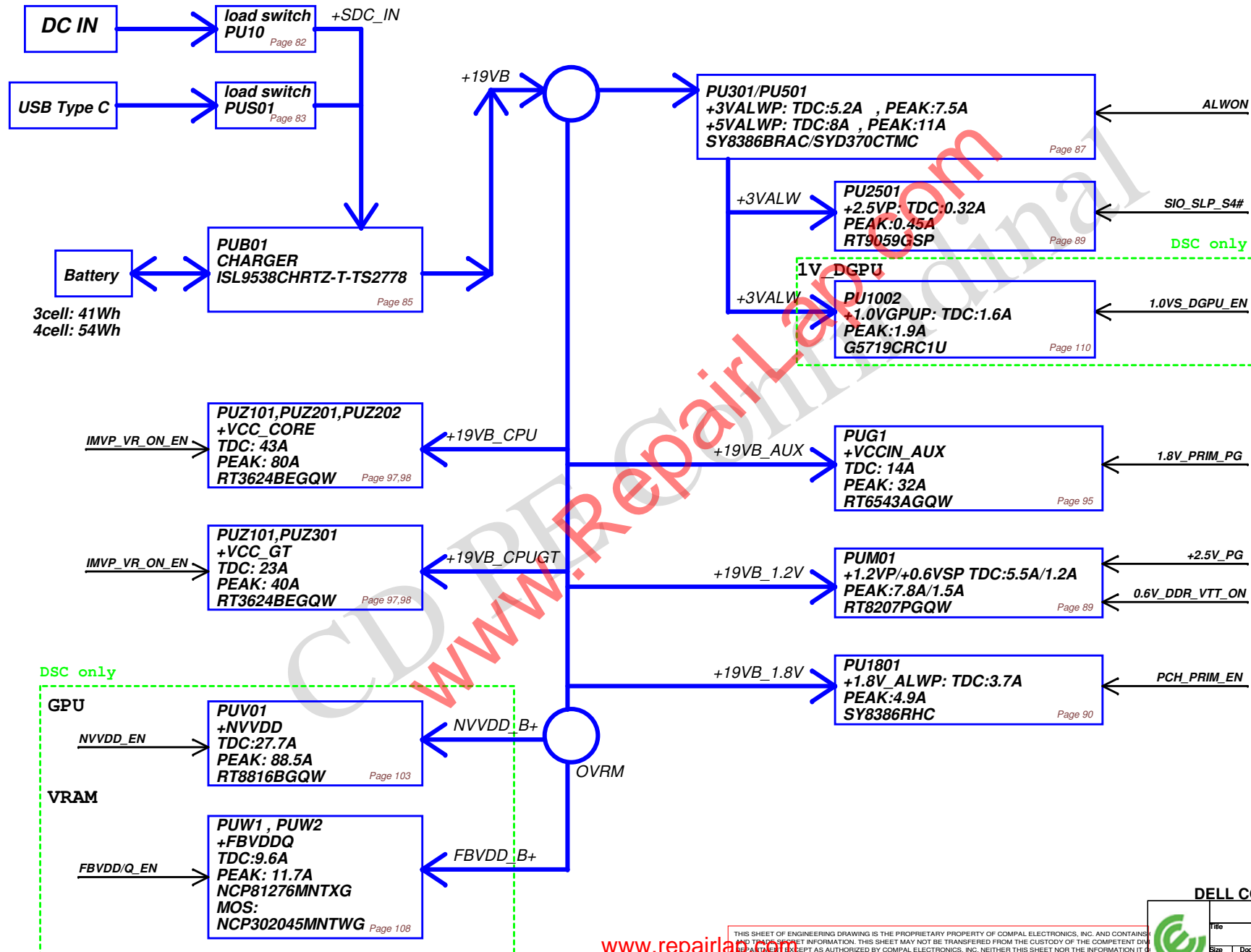
5		4		3		2		1	
D									
C									
B									
A									
5		4		3		2		1	

CD PE Confidential

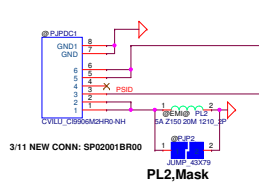
www.RepairLap.com

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								XDP	
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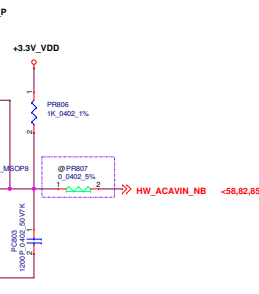
Power block



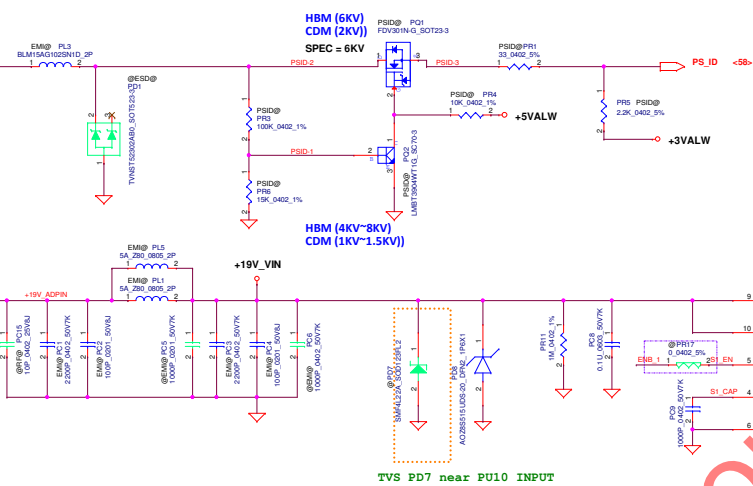
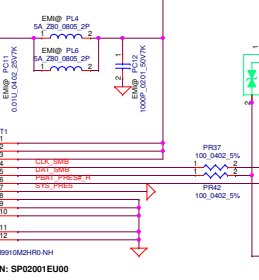
DCIN_AC_Power path



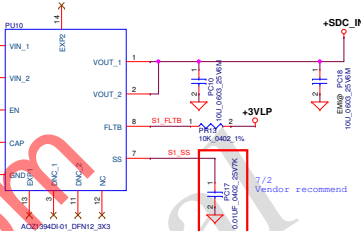
DCIN_AC_Detector



Battery Bot Side



S1



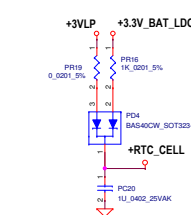
AOZ1394 High Active

DCIN1_EN	HW_ACVIN_NB	HW_ACVIN_NB
0	0	0
0	1	0
1	0	0
1	1	1

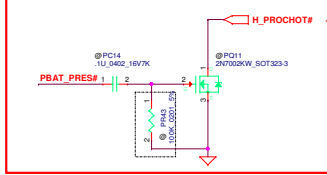
AOZ1394 High Active

depop for AOZ1394 High Active

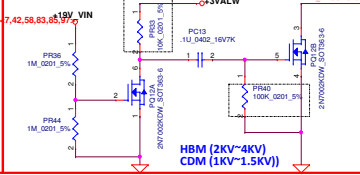
COIN RTC Battery



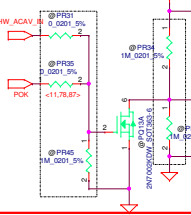
Battery unplug prochat
If battery removed, adapter only,
asserts H_PROCHOT# when adapter is
unplugged, keep low for 10ms
till SW PROCHOT# is issued by EC



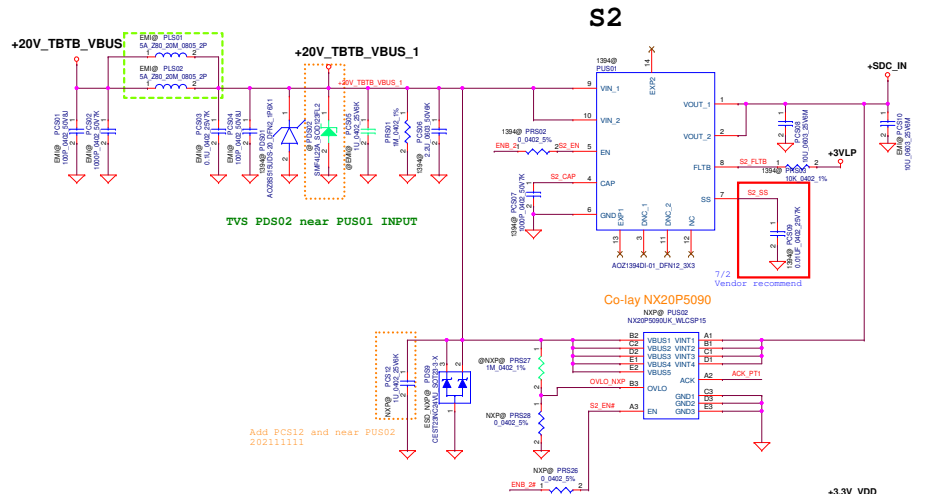
Adapter unplug prochat
asserts H_PROCHOT# when adapter is
unplugged, keep low for 10ms
till SW PROCHOT# is issued by EC



Erp lot6 Circuit



VBUS Power path



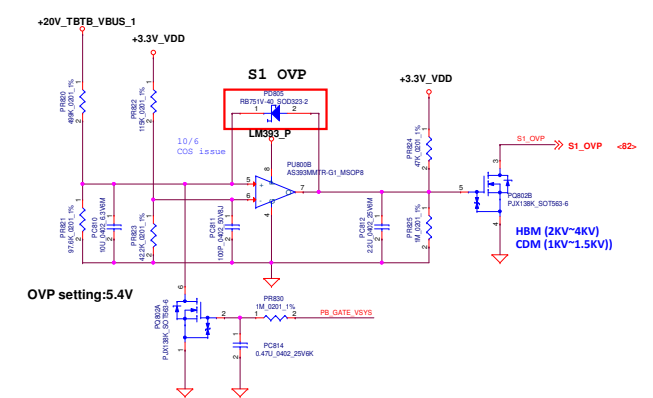
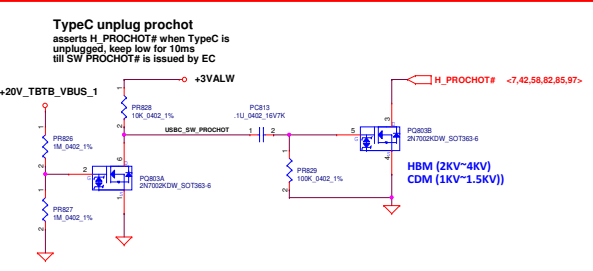
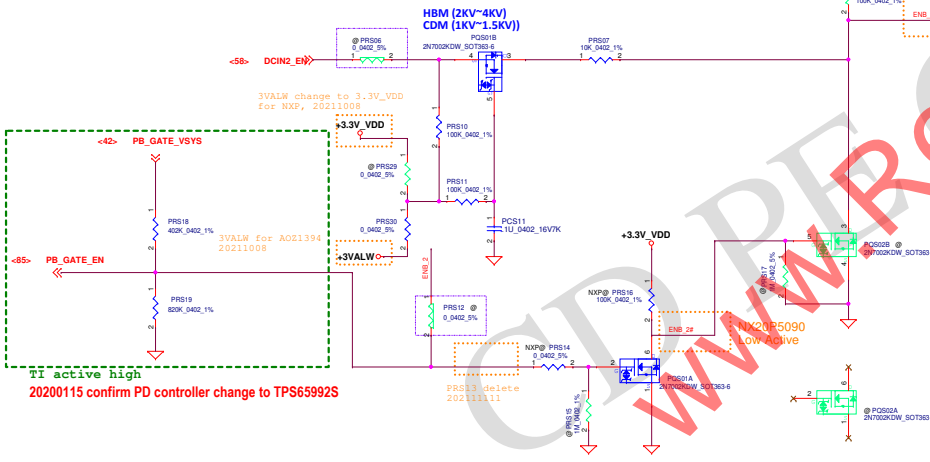
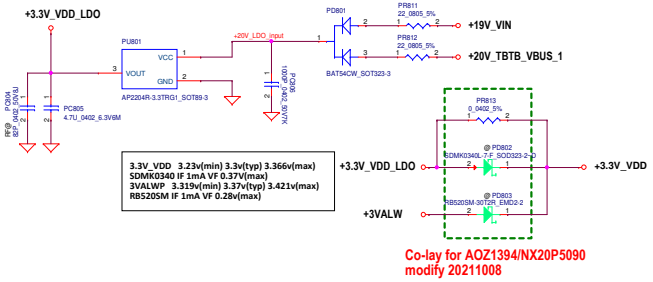
AOZ1394 High Active

DCIN2_EN	PB_GATE_VSYS	ENB_3
0	0	0
0	1	0
1	0	0
1	1	1

NX20P5090 Low Active

DCIN2_EN	PB_GATE_VSYS	ENB_3
0	0	1
0	1	1
1	0	0
1	1	0

PB_GATE_VSYS = 0, floating
DCIN2_EN default = 1, when EC has power on
20210924 confirm PD controller change for true value

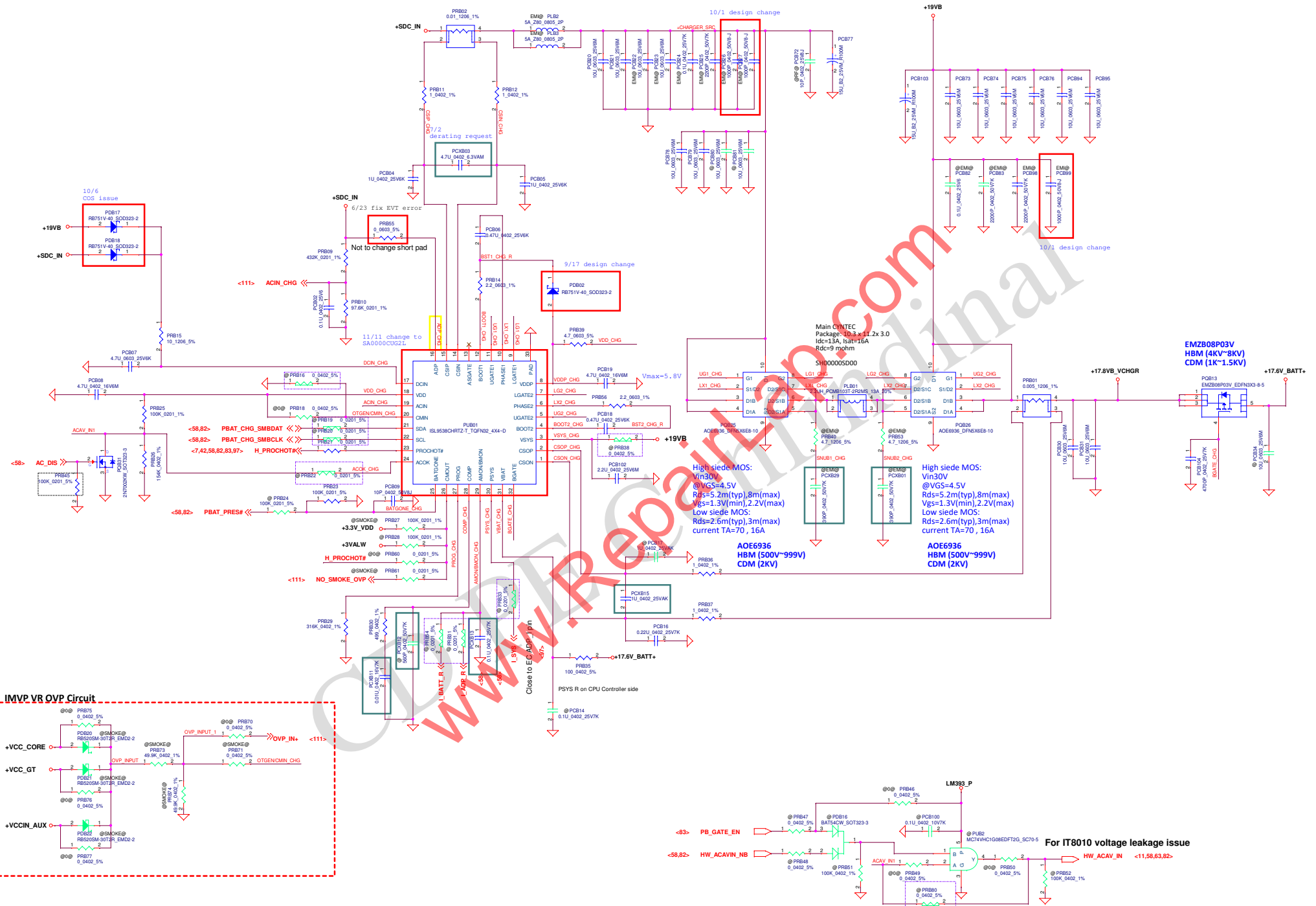


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Main Func = CHARGER

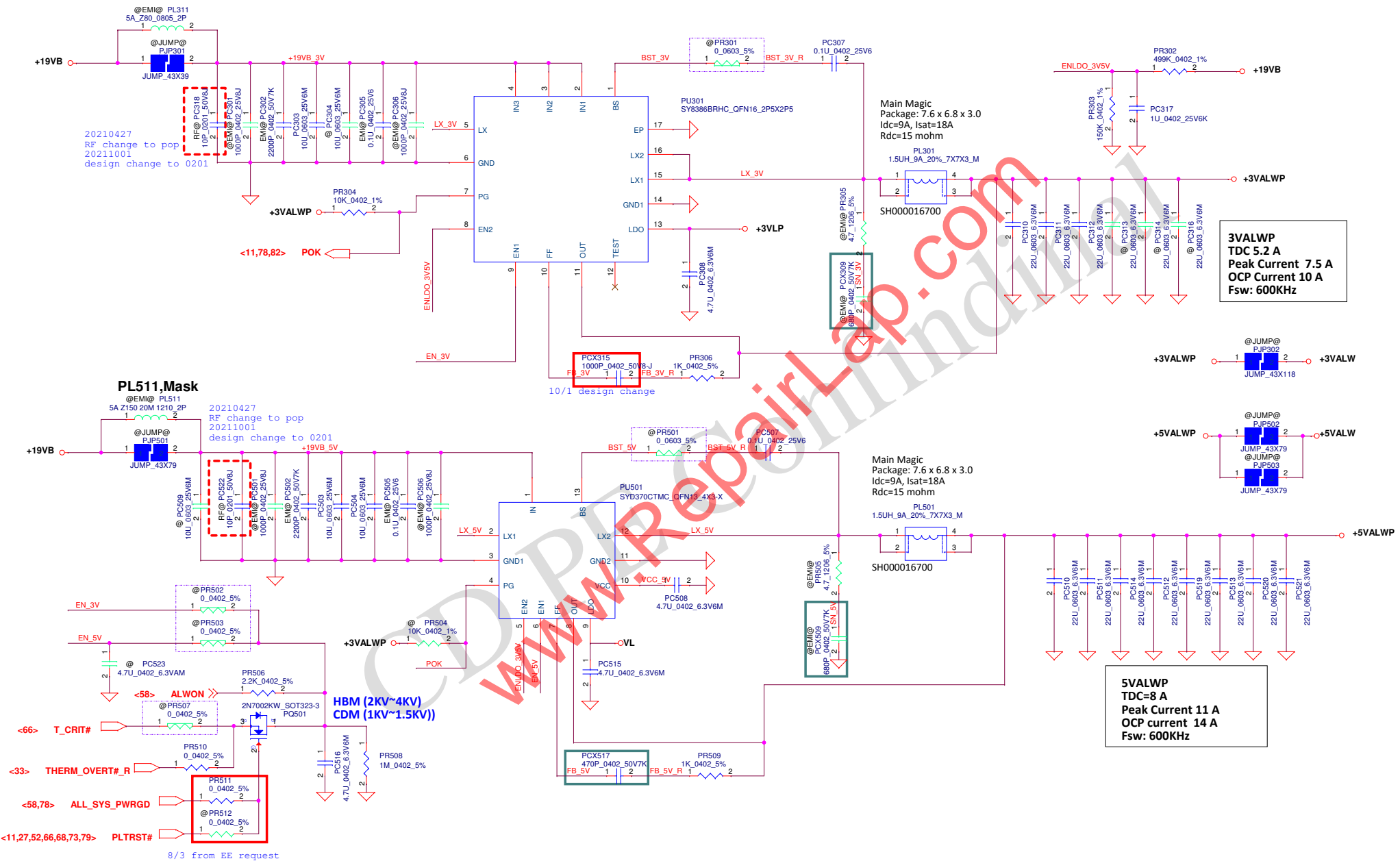


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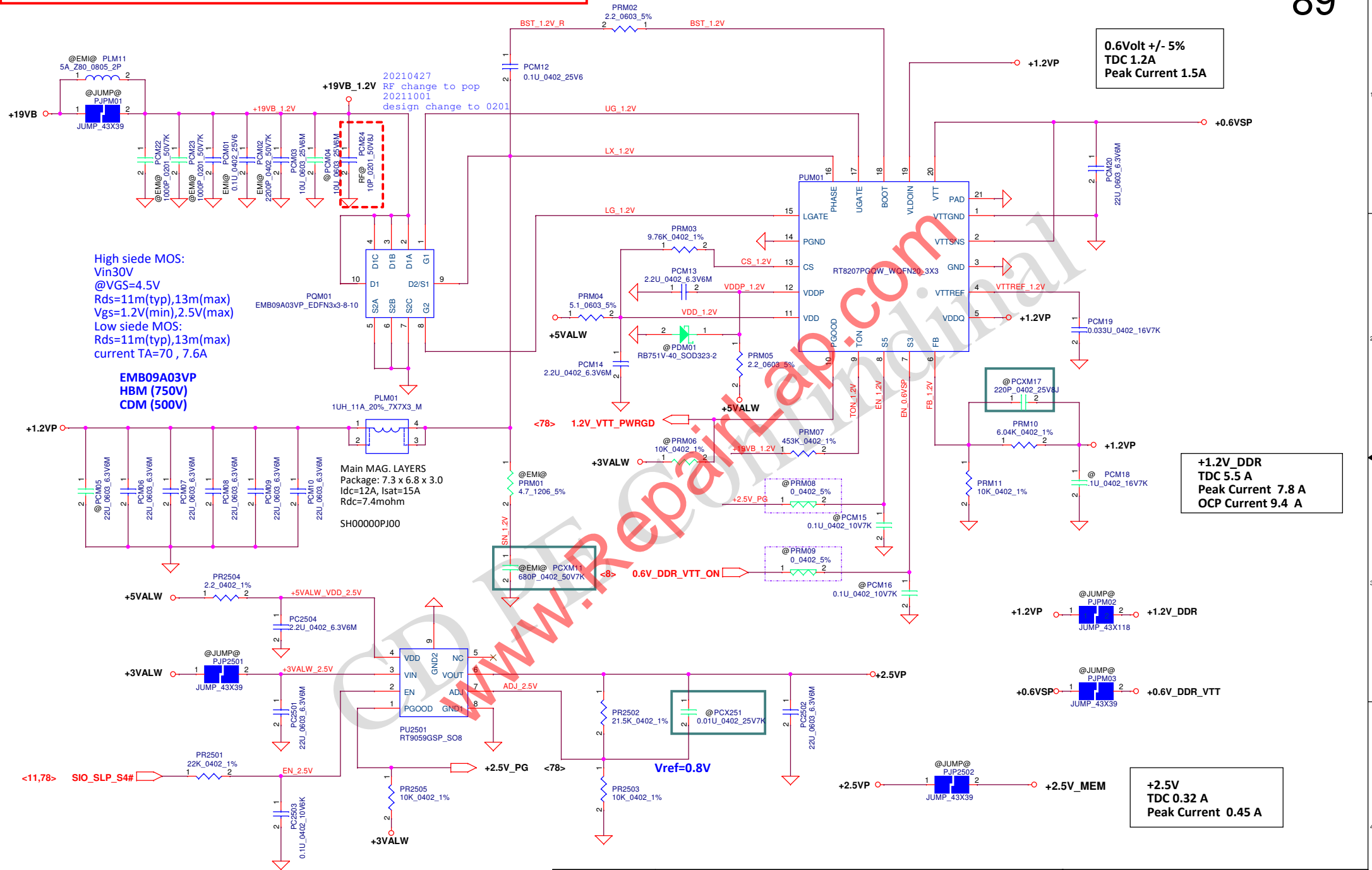
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				0.1	
				Date: Saturday, April 06, 2022	Sheet 88 of 121

Main Func = +1.2V_DDR/+0.6V_DDR_VTT/+2.5VP

89

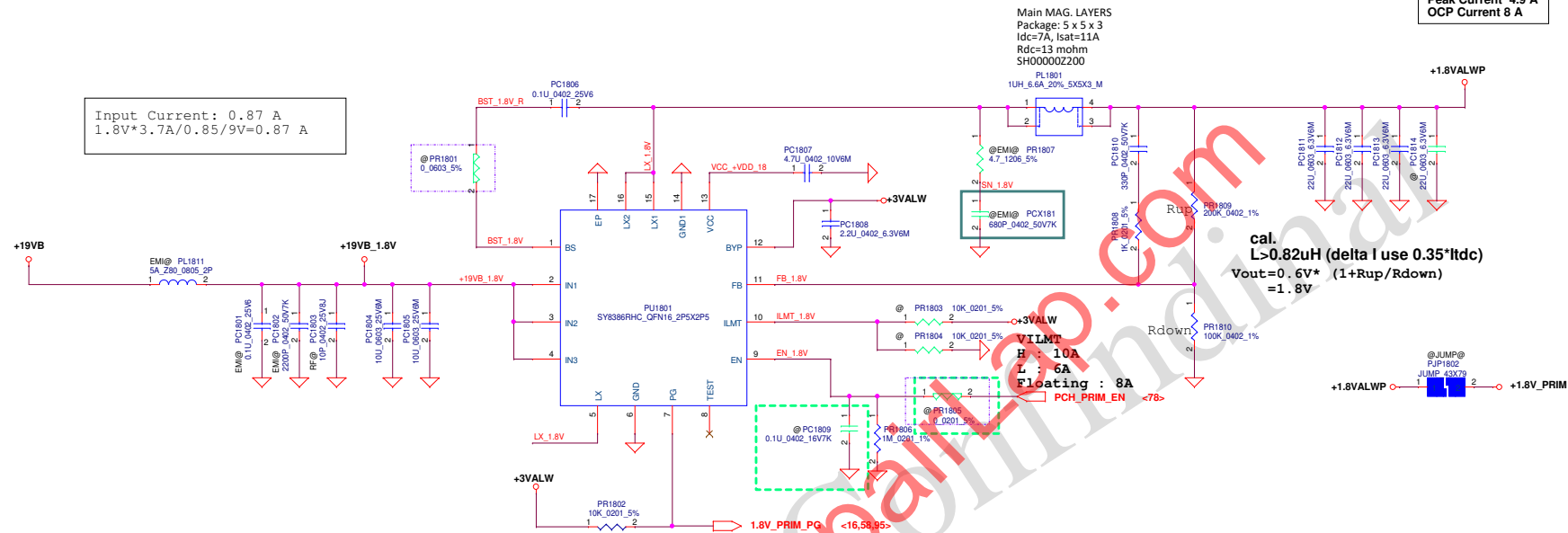


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The current limit is set to 6A, 8A or 10A when this pin is pull low, floating or pull high.

OCP setting	ILMT(pin3)
6A	Pull low
8A	Floating
10A	Pull high

Input Current: 0.87 A
 $1.8V \times 3.7A / 0.85 / 9V = 0.87 \text{ A}$



cal.
 $L > 0.82 \mu\text{H}$ (delta I use $0.35 \cdot I_{\text{ldc}}$)
 $V_{\text{out}} = 0.6\text{V} \cdot (1 + R_{\text{up}}/R_{\text{down}})$
 $= 1.8\text{V}$

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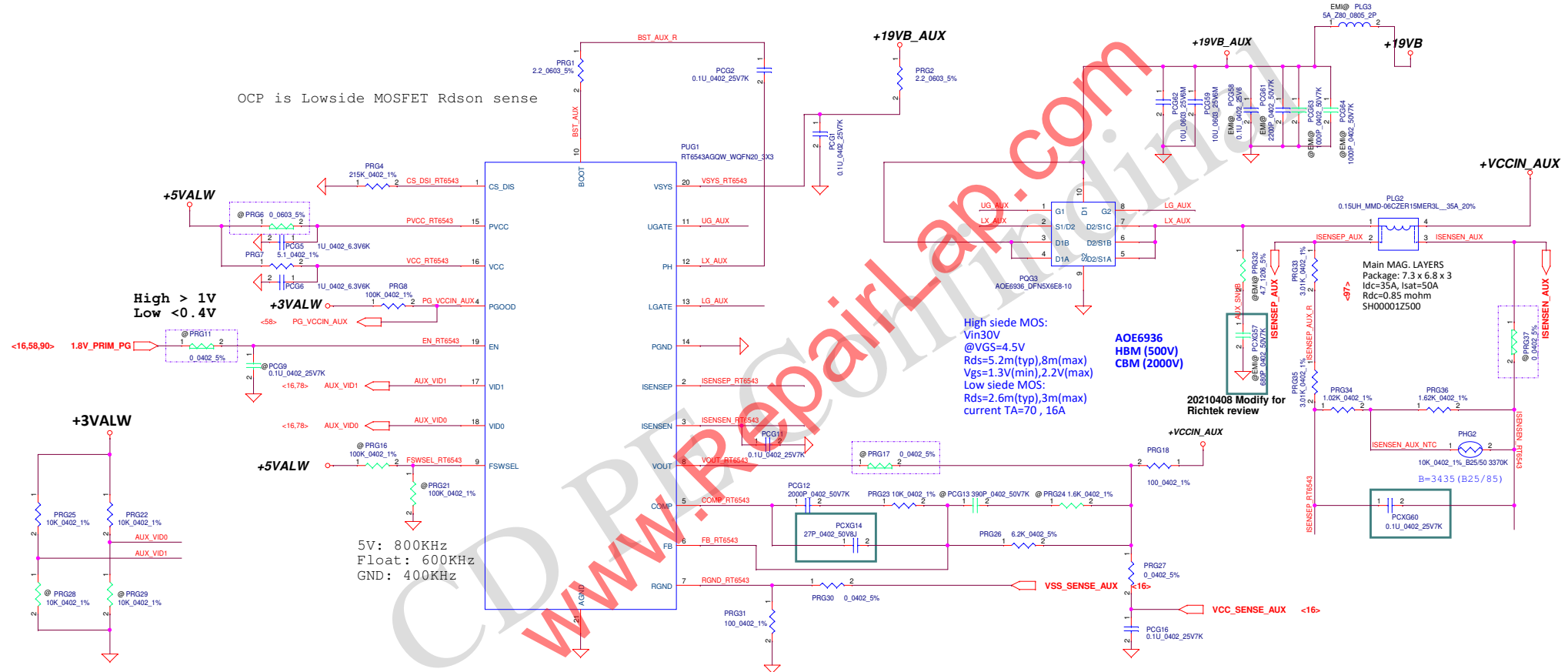
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TDC=14A
 ICCMAX=32A
 OCP=38.4A
 DC LL=2.0m ohm
 AC LL=3.4m ohm
 Fsw: 600KHz

OCP is Lowside MOSFET Rdson sense



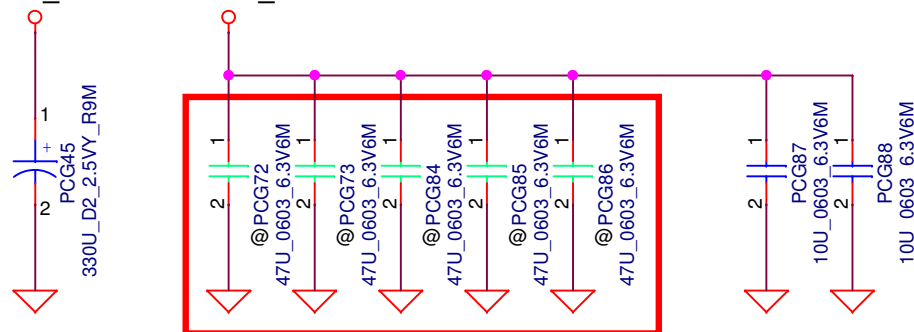
VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Main Func = VCCIN_AUX Decoupling

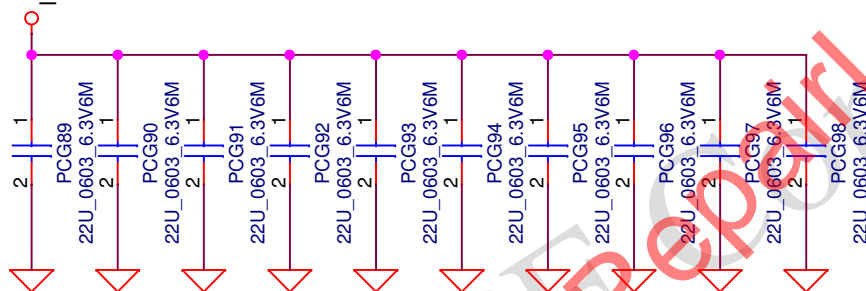
96

+VCCIN_AUX +VCCIN_AUX

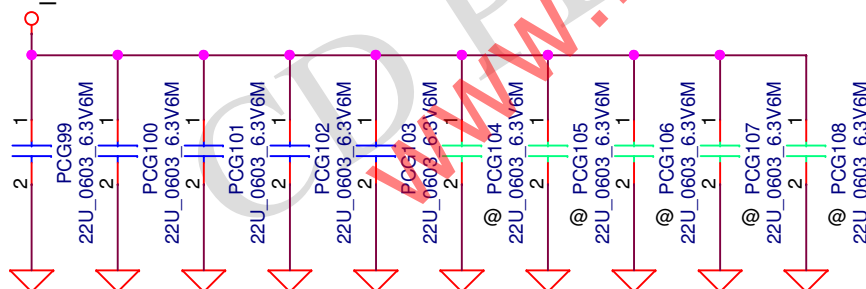


7/30 validation result

+VCCIN_AUX



+VCCIN_AUX



ADL-P_15W

+VCCIN_AUX

ICCMAX=32A

TDC=14A

OCP=38.4A

DC LL=2.0m ohm

AC LL=3.4m ohm

+VCCIN_AUX O/P caps:

330U_D2 2.5VM_R9M * 1pcs

10U/6.3V/X5R/0603 * 2 pcs

22U/6.3V/X5R/0603 * 15 pcs

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				Date:	Saturday, April 09, 2022

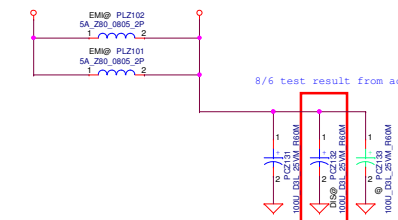
Compal Electronics, Inc.	
Title	
PWR VCCIN_AUX Decoupling	
Size	Document Number
	LA-L947
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Main Func = VCCIN

+19VB

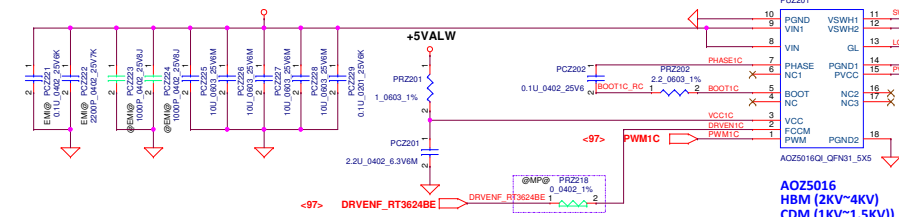
+19VB_CPU

8/6 test result from acoustic



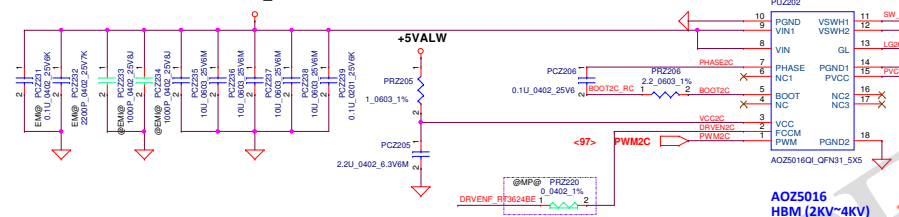
+19VB_CPU

+5VALW



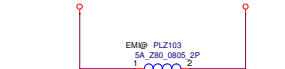
+19VB_CPU

+5VALW



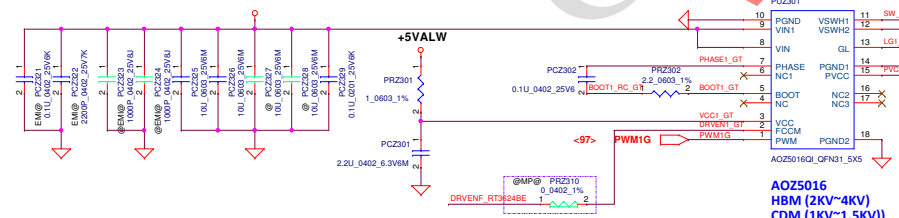
+19VB

+19VB_CPUGT



+19VB_CPUGT

+5VALW



ADL-P_15W

+VCC_CORE

+VCC_GT

+VCCIN_AUX

TDC=43A
ICCMAX=80A
OCP=96A
DC LL=2.8m ohm
AC LL=2.8m ohm

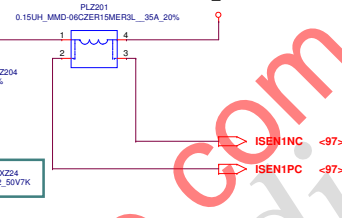
TDC=23A
ICCMAX=40A
OCP=48A
DC LL=3.2m ohm
AC LL=3.2m ohm

TDC=14A
ICCMAX=32A
OCP=38.4A
DC LL=2.0m ohm
AC LL=3.4m ohm

Switching Frequency= 600K Hz

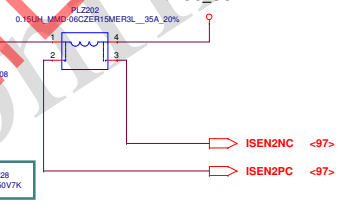
SH00001Z500
7*7*3
0.15uH
RDC=0.85 +/-5% ohm
Idc=35A
Isat=50A

+VCC_CORE



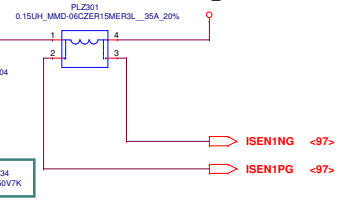
SH00001Z500
7*7*3
0.15uH
RDC=0.85 +/-5% ohm
Idc=35A
Isat=50A

+VCC_CORE



SH00001Z500
7*7*3
0.15uH
RDC=0.85 +/-5% ohm
Idc=35A
Isat=50A

+VCC_GT



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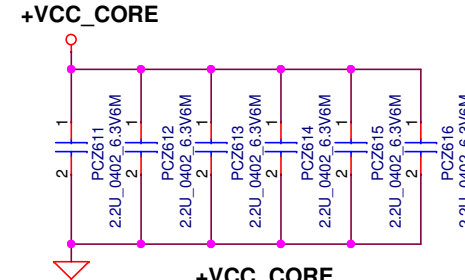
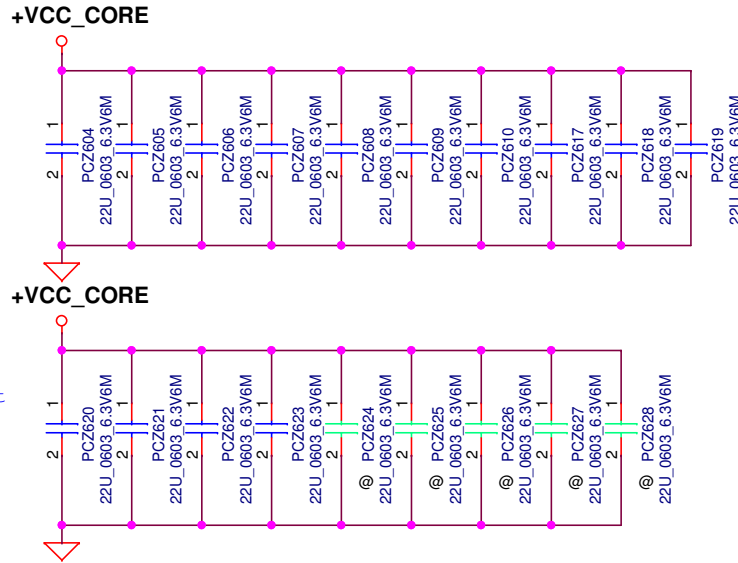
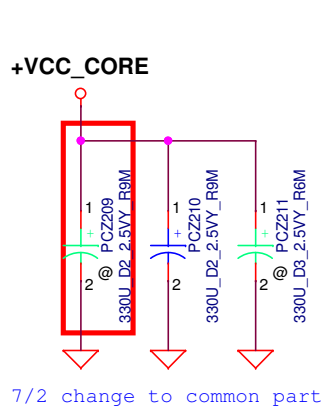
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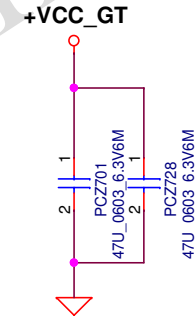
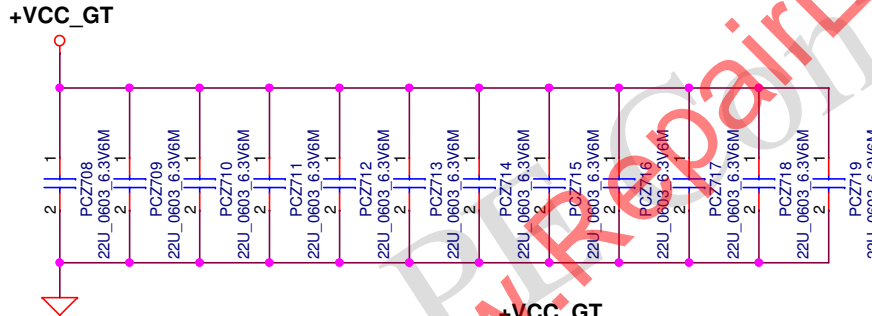
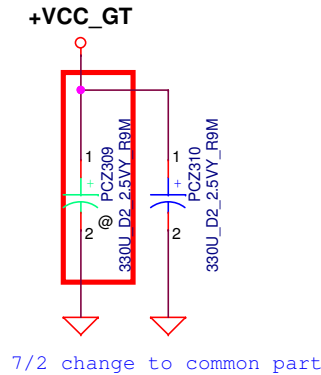
Main Func = VCCIN Decoupling

101



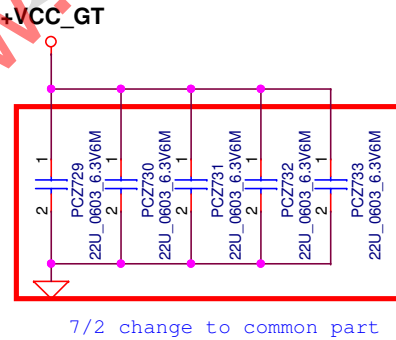
+VCC_CORE O/P caps:

330U_D2_2.5VM_R9M * 1pcs
47U/6.3V/X5R/0603 * 3 pcs
2.2U/6.3V/X5R/0402 * 6 pcs
22U/6.3V/X5R/0603 * 14 pcs



+VCC_GT O/P caps:

330U_D2_2.5VM_R9M * 1pcs
47U/6.3V/X5R/0603 * 2 pcs
22U/6.3V/X5R/0603 * 17 pcs



Function feild:
+VCC_CORE output cap:36.4
+VCC_GT output cap:36.5

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Main Func = GPU CORE Decoupling

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Under GPU Core

+NVVDD

1U 10V_0402/X6S * 8
10U_6.3V_0603/X6S * 25

+GPU_CORE (GN18-S5)
TDC=27.7A
Peak Current 88.5A
OCP= 105A

Near GPU Core

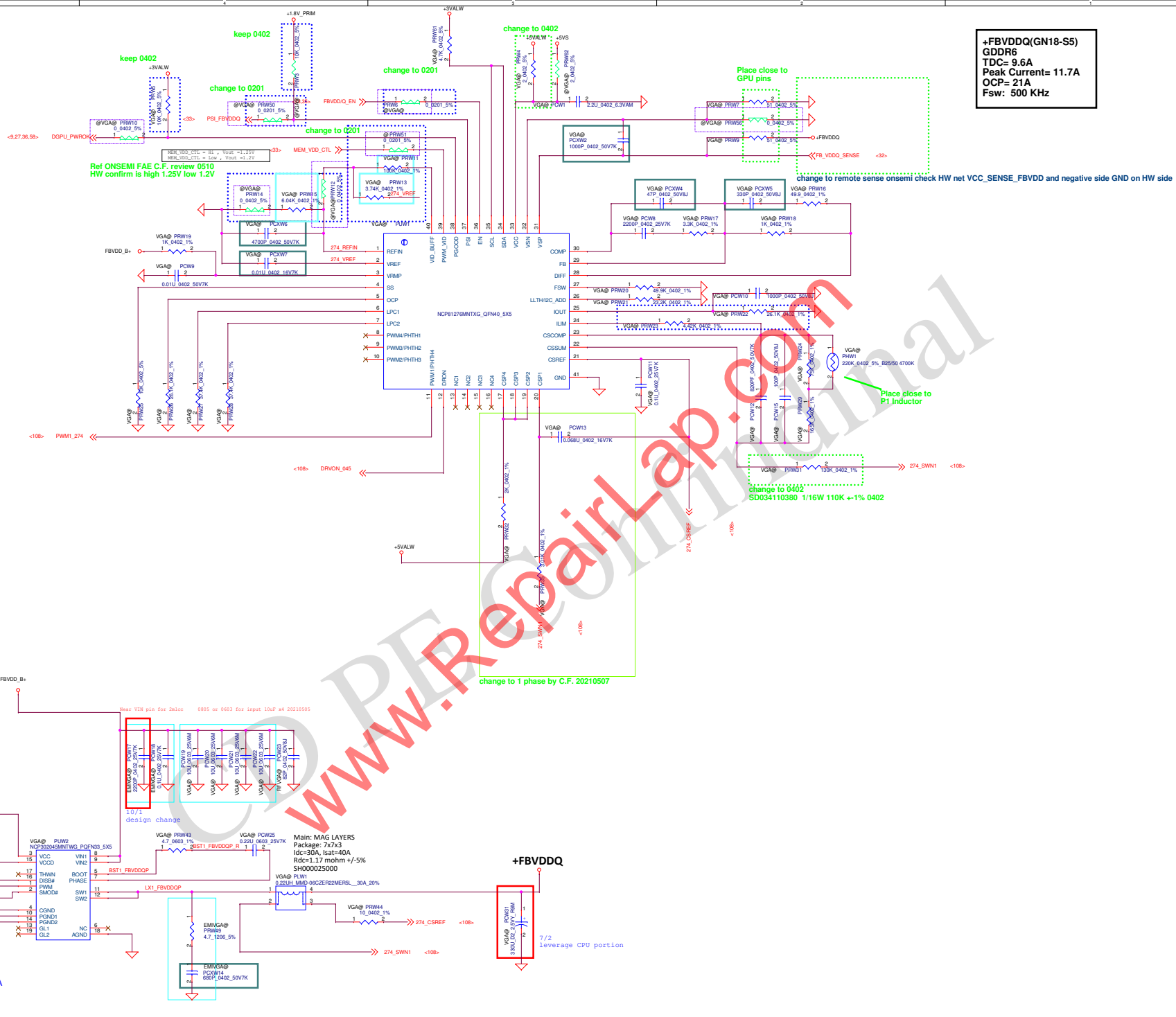
+NVVDD

330U 2.5V_R9M * 2
22U_6.3V_0603/X6S * 15
Reserve 22U_6.3V_0603/X6S * 2

+GPU_CORE (N17S-G5)
TDC=35A
Peak Current 78A
OCP= 93A

+GPU_CORE (N18S-G5)
TDC=32.6A
Peak Current 78A
OCP= 93A

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+FBVDQ(GN18-S5)
GDDR6
TDC= 9.6A
Peak Current= 11.7A
OCP= 21A
Fsw= 500 KHz

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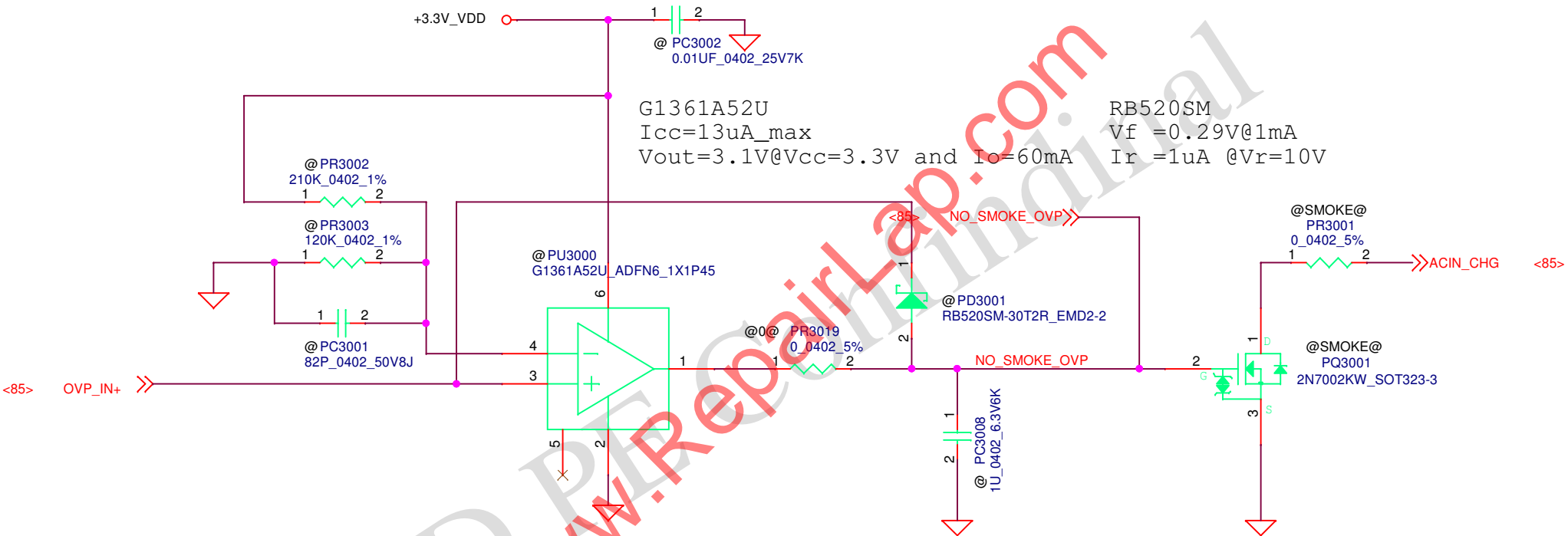
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SP-10296-001_v01_202102
+1.0VGPUP
GN18-S5-GDDR6
TDC: 1.6 A
Ipeak: 1.9A
Fsw: 1MHz

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$$V_f = 1.152V - 1.2V - 1.248V$$

1. +3.3V_VDD output accuracy +/-2%
2. R tolerance +/-2%



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1.	P097-VCCIN/GT (RT3624BE)	20210730	COMPAL	Intel validation result	change PRZ135 from 5.23k to 5.6k change PRZ138 from 5.23k to 5.36k change PRZ145 from 40.2k to 27k change PRZ146 from 15k to 10k change PRZ151 from 53.6k to 36k change PRZ152 from 15k to 10k	X01
2.	P101-+VCORE DECOUPLING	20210730	COMPAL	Intel validation result	unpop PCZ209,PCZ309 pop PCZ729,PCZ730,PCZ731,PCZ732,PCZ733	X01
3.	P096-VCCIN_AUX Decoupling	20210730	COMPAL	Intel validation result	unpop PCG72,PCG73,PCG84,PCG85,PCG86	X01
4.	P087-3.3VALWP/5VALWP	20210803	COMPAL	EE request	unpop PR512, pop PR511	X01
5.	P104-GPU_CORE-SW	20210806	COMPAL	Acoustic request for UMA only	unpop PCZ132 (UMA only)	X01
6.	P097-VCCIN/GT (RT3624BE)	20210806	COMPAL	Vendor recommend	add PCZ103 330p	X01
7.	P085-CHARGER (ISL9538C)	20210917	COMPAL	Avoid boot up issue	add PDB02	X02
8.	P097-VCCIN/GT (RT3624BE)	20211001	COMPAL	Change Psys setting value	change PRZ117 from 7.87k to 15.4k	X02
9.	P082-DCIN CONN/BATT CONN	20220207	COMPAL	change to short pad	unpop PR14,PR15,PR17,PR804,PR807	1.0
10.	P083-TYPEC	20220207	COMPAL	change to short pad	unpop PRS06,PRS12	1.0
11.	P085-CHARGER (ISL9538C)	20220207	COMPAL	change to short pad	unpop PRB16,PRB38,PRB80,PRB19,PRB20,PRB22,PRB31,PRB54	1.0
12.	P087-3.3VALWP/5VALWP	20220207	COMPAL	change to short pad	unpop PR301,PR501,PR502,PR503,PR507	1.0
13.	P089-+1.2V/+0.6V/2.5V	20220207	COMPAL	change to short pad	unpop PRM08,PRM09	1.0
14.	P090-+1.8V	20220207	COMPAL	change to short pad	unpop PR1801,PR1805	1.0
15.	P095-VCCIN_AUX (RT6543)	20220207	COMPAL	change to short pad	unpop PRG6,PRG11,PRG17,PRG37	1.0
16.	P097-VCCIN/GT (RT3624BE)	20220207	COMPAL	change to short pad	unpop PRZ124,PRZ128,PRZ129,PRZ130,PRZ134,PRZ143,PRZ147,PRZ149,PRZ153,PRZ163,PRZ164,PRZ168,PRZ200	1.0
17.	P098-VCCIN-SW	20220207	COMPAL	change to short pad	unpop PRZ218,PRZ220,PRZ310	1.0
18.	P103-GPU_CORE (RT8816B)	20220207	COMPAL	change to short pad	unpop PRV04,PRV06,PRV15,PRV16,PRV17	1.0
19.	P108-GPU_VRAM (NCP81276)	20220207	COMPAL	change to short pad	unpop PRW10,PRW12,PRW14,PRW56,PRW6,PRW50,PRW51	1.0

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